OSI

OHIO SCIENTIFIC INSTRUMENTS

HAYDEN STREET, HIRAM, OHIO 44234

OSI 440 Video Graphics Board

Introduction

The 440 Video Graphics Board is an extremely versatile television display interface. It can be used as an alphabetic display and can have graphics and color capability. The board also features a keyboard input latch to minimize the board count in starter systems. The most basic application of the board is as an alphabetic display. The board will display up to 32 rows of 32 ASCII characters on a video screen. The characters are generated by a 2513 character generator ROM in the standard 5 by 7 dot matrix font. The character set is the standard 64 character teletype set. Thus, only 6 bits are required to define a character. Each of the 1,024 characters which is displayed constantly corresponds to a memory location in the 1,024 byte on-board memory. This 1K memory is treated as normal read/write RAM memory by the processor. Thus, the ASCII equivalents of the data stored in these locations will constantly be displayed on the video screen. The processor has complete random access capability to any point in the memory and, therefore, the screen, and can transfer data in and out of this memory very rapidly (over 100,000 bytes per second). The screen is over ten times faster than the fastest conventional CRT display! (9600 baud) This feature allows real-time animation of the display.

The 440 board itself can not provide carriage return, line feed, cursor control or even memory load functions stand-alone, but requires software for these functions. The simplest teletype-like functions can be obtained with a very simple program which poles a keyboard, deposits the keyboard data in a display memory location and moves on to the next

memory location. This program would simply display messages on the screen with no control functions. Blanks would be generated with the ASCII space and an automatic carriage return line feed would occur every 32 characters.

A software line feed could be added by adding 32 to the memory "pointer" whenever an ASCII line feed is encountered. Similarly, carriage return, cursor control, character blink, scrolling, and all other conventional functions can be obtained because the display has the full intelligence of the processor available. OSI CRT simulator software performs these functions.

Color (Optional)

Since the character generator only utilizes six bits to define a character two bits are free for other purposes. One bit could be used to invert the character (black on white), but, a more interesting use is to utilize the two bits to select one of four colors for each character location. For example, each character could be white, red, yellow, or green (blue generally has poor visibility). Any graphics within the character cell would be the same color also. This user addition is discussed later in the manual.

Graphics (Optional)

Each 5 by 7 character is boardered by three rows of dots and one column of dots so that each character "cell" has 8 by 8 dots. This corresponds to 256 rows by 256 columns of dots or 65K dots. It would be nice to be able to access any of these dots but, it would require 8K bytes of very fast memory to be able to do so. Furthermore, this dot pattern is near the limits of resolution of a normal T.V. set

and a microprocessor is too slow to utilize such a large array for real time animation. Consequently, the next smallest array (128 by 128) is utilized in the graphics option to the 440 board.

This requires 16K bits or 2K bytes of memory which are located on a dedicated 420 Memory Expansion Board. The dedicated memory board communicates with the 440 board via ribbon cable instead of the backplane. However, it still occupies a slot on the backplane board to obtain power. This 2K memory again is treated as conventional memory by the processor, but, each bit of the memory corresponds to a four dot square on the screen. The graphics are super-imposed on the alphabetic display and are affected by the color control if installed. Consequently, very spectacular video displays can be generated.

Theory of Operation

The Model 440 Video Graphics Board appears identical to a 420 Memory Expansion Board to the computer system. The board uses the same address decoding control and data buffer circuitry as the Model 420 Board.

When the board is not being accessed by the processor, it is in the display mode and is constantly automatically displaying the contents of its memory on a video screen. When the processor accesses the board for a conventional read/write operation, the display process is interrupted and the board goes into its memory mode. In fact, the board can be used as a conventional memory for program and/or data storage. Diagram A is the block diagram for the board. Each functional block will be discussed in detail.

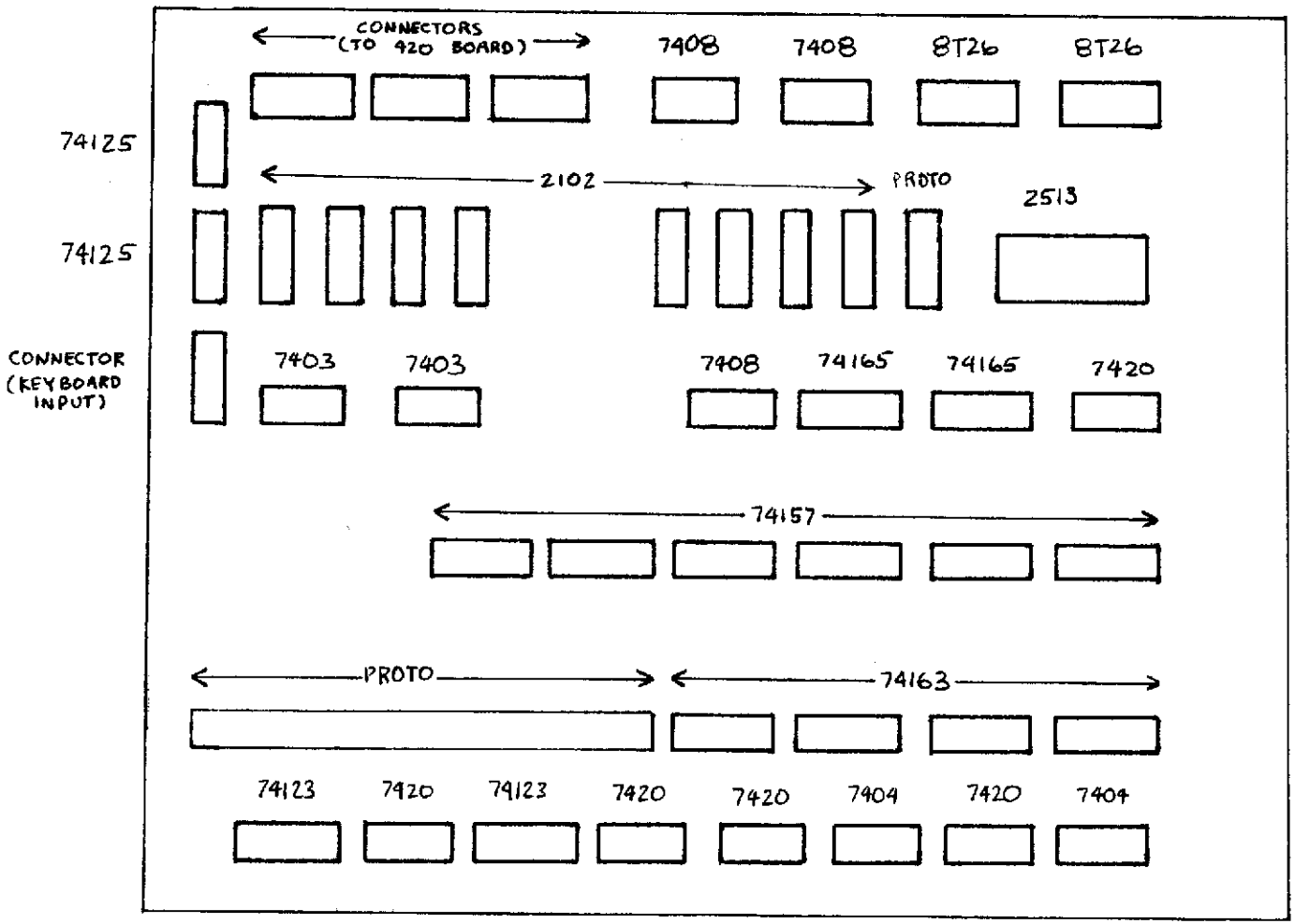


Diagram A. 440 Board Layout

Board Selector and Decoder

Diagram B shows this ciruitry. The upper address bits are inverted and can be jumpered to a four input gate to select the board Thus, the board occupies 4K of memory space and can be located at any of the 16 4K locations (DXXX is recommended). A_{11} and A_{10} are used to further decode four 1K memory enable signals which are gated with Ø2·VMA. $\overline{CEA}$ is used to select the 1K apphabetic memory. $\overline{CEB}$ and $\overline{CEC}$ are used for the 2K graphics memory and $\overline{CED}$ can be used for 1K of non-displayed memory or to enable the on-board keyboard indput. R/W, Ø2·VMA, and BE (board enable) are gated to control the direction of the 8T26 data buffers on board and the data direction line back to the processor.

Video Clocks

Three one shot timing circuits are used to control the display circuitry. These circuits have a wide adjustment range to acommodate different display formats. Consider conventional T.V. display first. A conventional low cost T.V. set should be run at exactly 60 frames per second or an objectionable shimy or hetrodyning will occur due to the direct 60 Hz leakage into the set. The free running horizontal frequency of a T.V. set is 15750 Hz. The video signal must meet these two criteria to be displayed on a T.V. set. Normal T.V. sets over-scan somewhat so that the edges of the display will not be usable. Last, but not least, is the bandwidth capability of the set. Most portable sets can barely resolve 256 lines, making a 32 by 32 character display the largest practical on a conventional T.V. set.

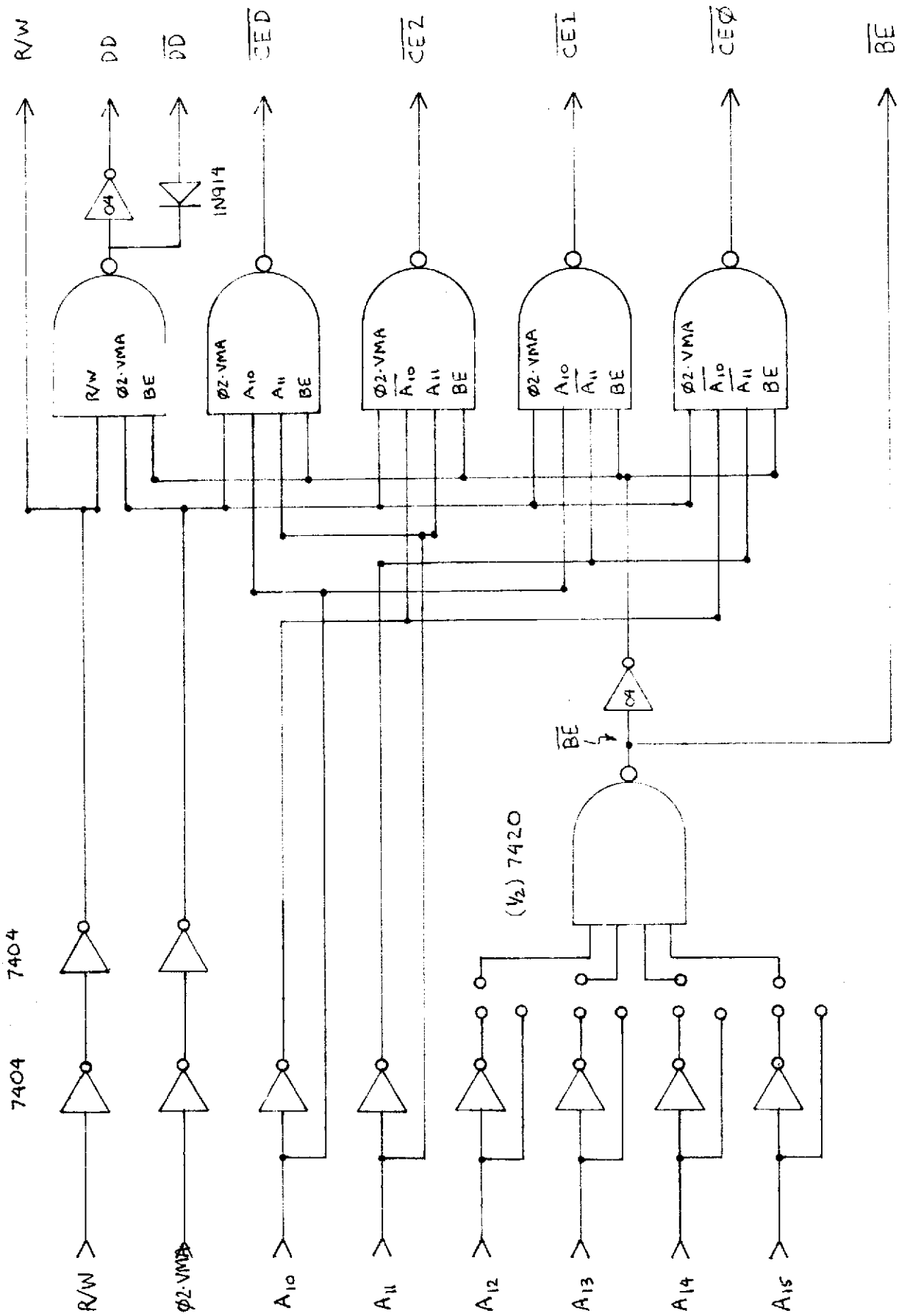


Diagram B. 440 Board Address Decoding

With this information in mind, consider Diagram C. A 74123 dual monostable is used as the basic system clock. It is adjusted to produce a nearly symmetrical square wave with a period from 200 to 400 nanoseconds (256 nanoseconds for 60 Hz).

A second 74123 is used to generate the horizontal and vertical sync and retrace blanking signals. The horizontal sync and vertical sync signals can be used to gate the output of the clock so that the entire field of 32 by 32 can be displayed. However, when a conventional T.V. set is used, over-scanning is present and a highly stable 60 Hz frame rate is desired. Consequently, the horizontal sync and the vertical sync signals would not gate the clock in this case. This will cause the loss of the first row and column on the display, but with overscan, it wouldn't be seen anyway. Also, only one element, the video clock, is controlling all the display timing. A trimmer pot can be brought out to the case to keep the clock in tune with the power line. Each frame is now .0166 seconds long. Each line is .0166/256 = 65 usec. long. Each character is 2usec. long and each dot is 128 nsec. long. The vertical sync and horizontal sync one shots are simply adjusted to eliminate retrace lines in the picture. This also greatly simplifies the intial set up.

If a video monitor is used, the 60 Hz problem should be greatly reduced. Furthermore, it should be possible to underscan the display so that the edges are visible. For this application, horizontal sync and vertical sync would gate the clock. This will result in a lower frame rate and less frame rate stability, but, will allow full 32 by 32 display.

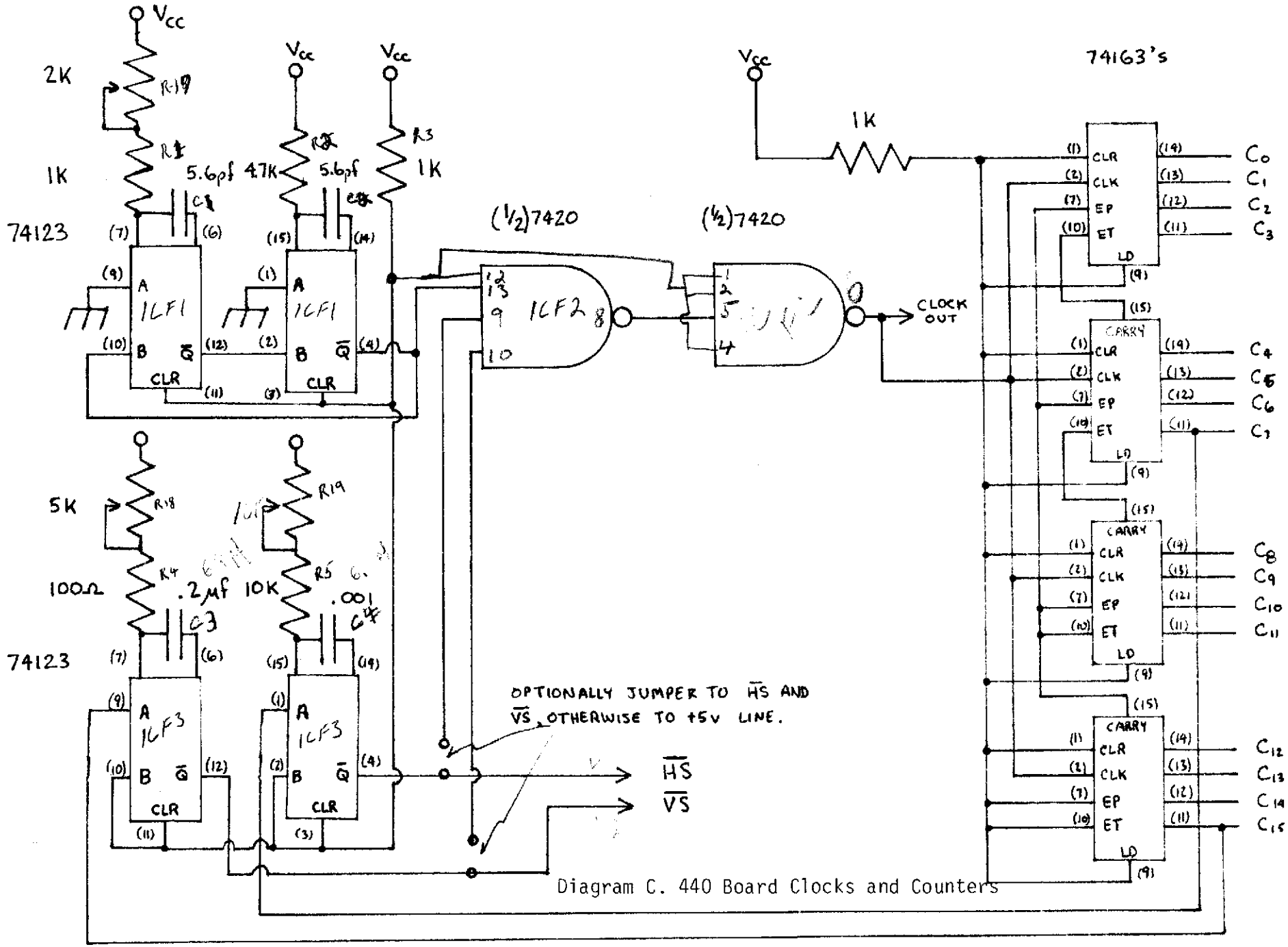


Diagram C. 440 Board Clocks and Counters

Counters

The video clock feeds a 16 bit synchronous counter (Diagram C) which is the heart of the display. Each "count" of this counter corresponds to one of 65K dots on the screen. The 8th bit of the counter triggers the horizontal one shot, generating 256 dot rows. The 16th bit triggers the vertical one shot generating 256 column frames. Other counter lines go to the memories, character generator, and shift registers.

Multiplexer

The counter lines to the memory addresses go through the 24 channel multiplexer as shown in Diagram D. The mutiplexer changes the mode of the board from display to memory whenever the board is selected by the processor. In the memory mode, the standard bus control and address signals are fed to the memories. In the display mode, the counter lines are fed to the memories. The addresses are constantly incremented in step with the display.

Alphabetic Memory

Diagram E shows the six to eight 2102 memories which store the ASCII code for the alphabetic display. Also shown are the connections to the optional graphics memory. All address and control lines are fed from the multiplexer. Data inputs are via the 8T26 buffers. Data ouputs are fed to the character generator (alphabetic memory), the graphics shift register, and a data multiplexer (See Diagram E). The data multiplexer combines the direct output of the alphabetic memory, graphics memory, and optional keyboard input to feed the 8T26 data buffers. The 8T26 buffer configuration is standard to all system boards and will not be discussed here.

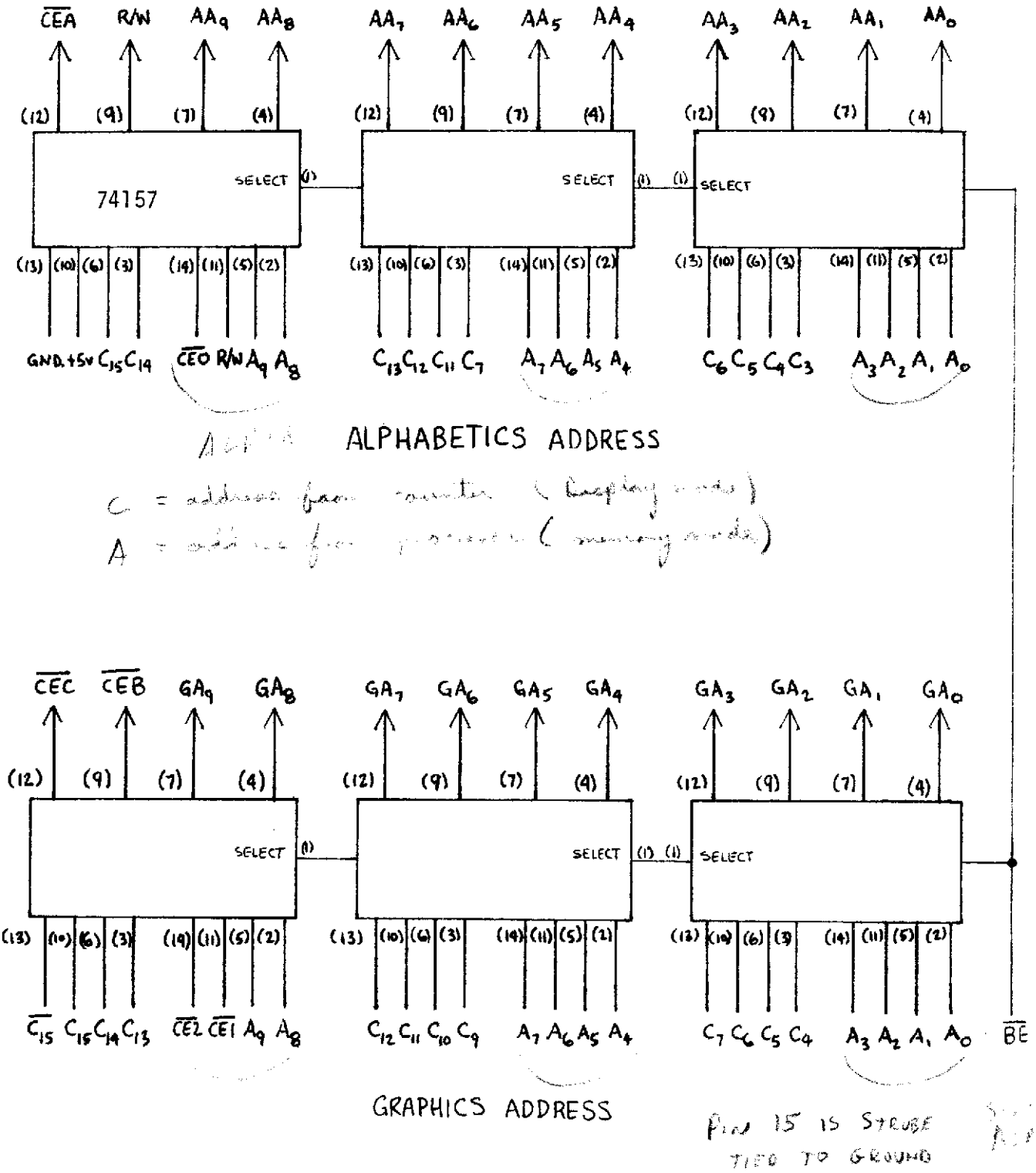


Diagram D. 440 Address Multiplexer

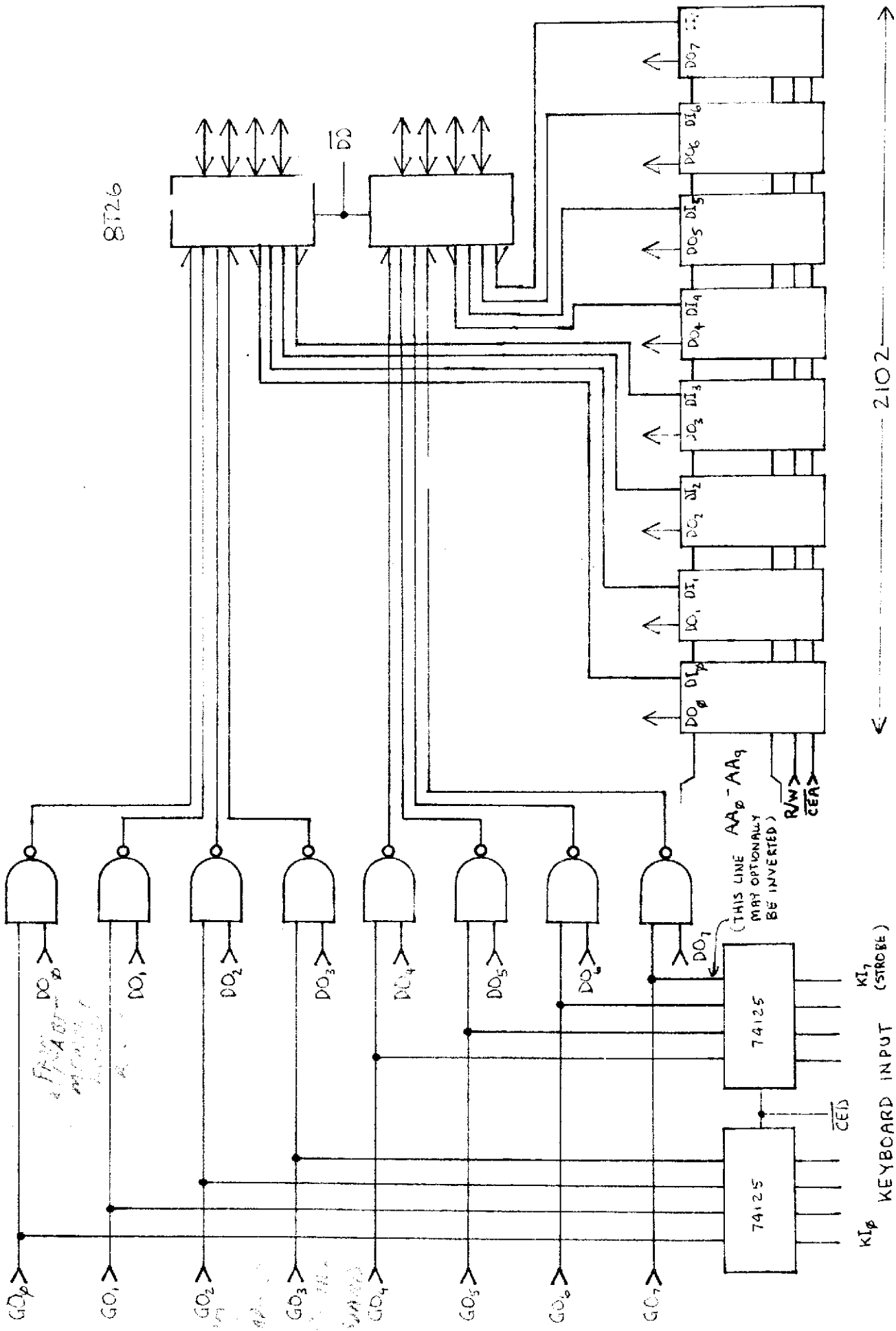


Diagram E. 440 Alphabetics memory, data multiplexer, and data buffers

Character Generator

The 2513 character generator ROM contains the codes for the 64 character 5 by 7 font used by the display. The ROM actually has a 5 by 8 capability but the bottom row is always blank. Diagram F shows the ROM's implementation on the 440 board. Six data lines from the memories act as address lines to select a character. The character selected corresponds to the ASCII code on these lines. Three row select lines are brought in from the counter allowing the selection of eight different rows for each character. The five columns are outputed in parallel. To read out a character in a 5 by 8 dot matrix format, the proper ASCII code is first fed in the six address lines. Then the row address lines are cycled from 0 to 7 sequentially, yielding eight rows of five columns at the outputs. In actual operation on the 440 board, the first row of each of the first 32 characters is read out, then the second row, etc. until all eight rows are read out. The process then starts over for the next 32 characters until all 1,024 characters are read out. The process then repeats itself.

Alphabetic Shift Register

The five column outputs from the character generator are fed into a 74165 eight bit parallel load shift register. The inputed data is latched at the 8th column of each character so that the shift register is actually one character behind the rest of the system at all times. This feature allows one full character for memory and ROM access or approximately 2 usec. for alphabetics and 4usec. for graphics. The three high order inputs to the shift register are held low to generate the three blank columns after each character.

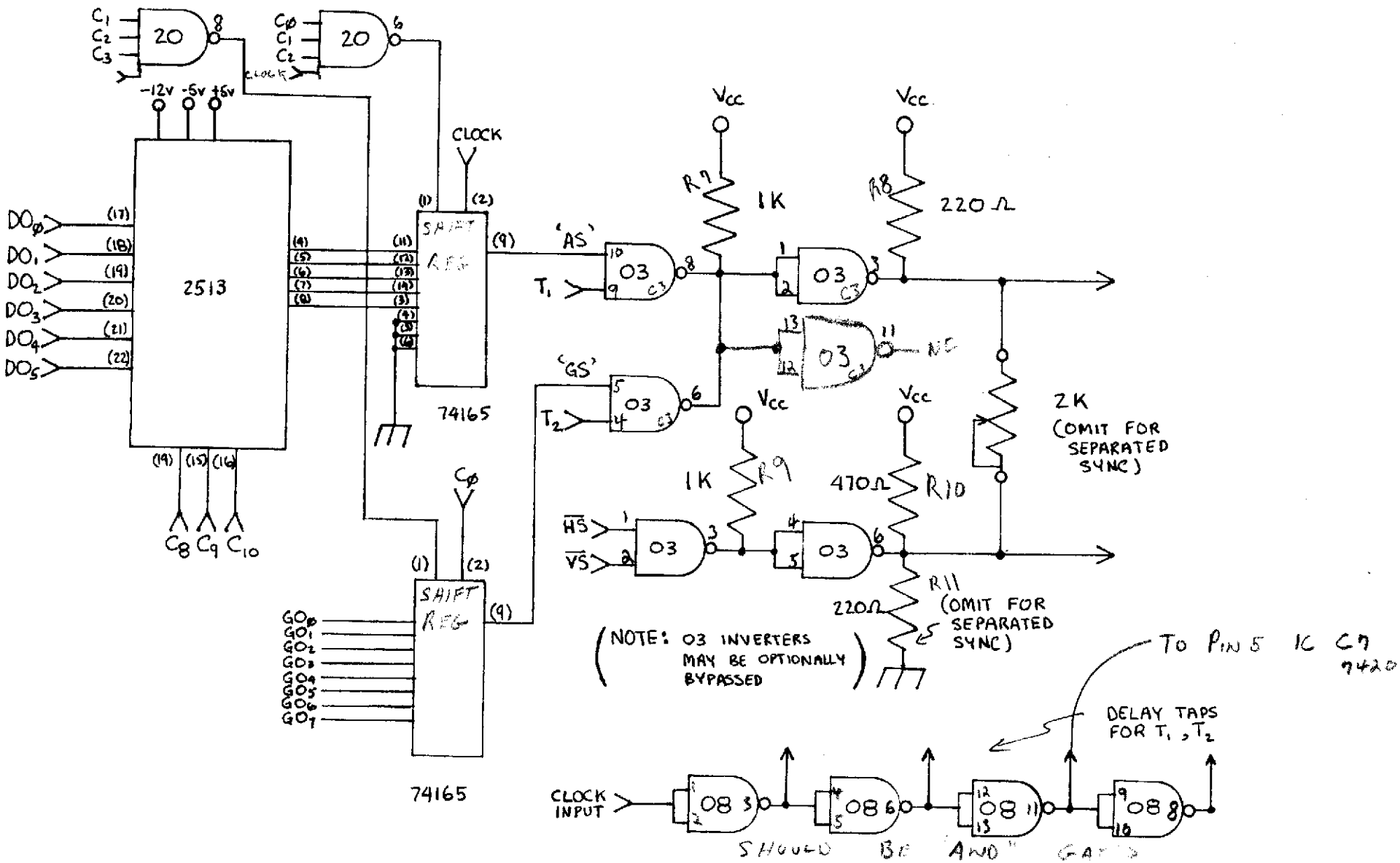


Diagram F. 440 Character generator shift register and video output

Graphics Shift Register

As per Diagram F, the eight data outputs of the graphics memory are fed to the parallel inputs of a second 74165 shift register. This shift register is clocked at one half the frequency of the other shift register producing dots twice as long. The data is loaded on the 8th column of this display or only one half as often as the other shift register.

The outputs of the two shift registers are open collector or'ed via 7403s. The outputs can be optionally gated with the system clock to produce sharp dots. If this gating is not done, rows of dots will run together to form lines. This may or may not be objectionable to the user. An additional stage of inversion is available for regular or inverted video. The $\overline{HS}$ (horizontal sync) and $\overline{VS}$ (video sync) signals are combined to form the sync signal. For separate sync operation, the sync signal and the video signal would be used in this form. For composite video, the signals are resitively mixed via open collector gates. A pot is available to vary the video contribution or contrast. The circuit shown here is optimized for use with the ATV Research "Pixie Verter" RF transmitter which can be mounted on the board!

WARNING:

The video output from this board should never be directly connected to a television set. Most T.V.s will require an isolation transformer for operation. Note also that most modern color sets have transformers which do not isolate from the line.

OSI MODEL 446 PARTS LIST

For Alphabetics Use Only

___ 1 - 440 Video Graphics Board
___ 2 - 7403
___ 2 - 7404
___ 3 - 7408
___ 5 - 7420
___ 2 - 74123 Texas Instruments or ITT units only.
___ 2 - 74125
___ 3 - 74157
___ 4 - 74163
___ 1 - 74165
___ 2 - 8T26
___ 1 - 2513N CM 2140 font recommended. Use ONLY Signetics Units.
___ 6 - 2102 type memories. "zero data hold time" 650ns. worst case for 1MHz operation, 350 ns. worst case for 2MHz operation.
___ 1 - 1N914

NOTE: Use only standard TTL since propagation delays are important

Resistors All ¼Watt 10% or Better

___ 4 - 220 ohm
___ 1 - 470 ohm
___ 7 - 1K
___ 1 - 2.2K
___ 2 - 4.7K
___ 1 - 10K
___ 2 - 5K pots
___ 1 - 10K pots

Capacitors 10V. Rating or Better 20% Tolerance

___ 1 - 6.8pf NPO (temperature stable)
___ 1 - 68pf NPO (temperature stable)
___ 1 - .001uf
___ 1 - .1uf stable (mylar or polycarbonate)
___ 1 - 25uf (optional)
___ 18- .1uf bypass capacitors

Graphics Parts Included in 446 Kit

___ 3 - 74157
___ 1 - 74165

Required Parts Not Supplied in 446 Kit

___ Sockets: at least one at keyboard connector
___ 4 - Female Molex Connectors
___ Jumper Wire
___ Solder

Required Parts for Graphics Not Supplied by OSI

___ 1 - 420B or 420C Memory Board
___ 16- 2102 Memories; specifications as above
___ 3 - Sockets (minimum)
___ 3 - 4" or longer 16 pin jumper cables
___ 1 - Female Molex Connector
___ Approximately 8 - Bypass Capacitors (.1uf)

The 440 video board has several jumperable options and tremendous expansion capability. However, its major use is as an alphabetics "terminal." The following instructions "set up" the 440 for general purpose use with alphabetics only or alphabetics and graphics with either a standard TV set or closed circuit monitor. The OSI Systems Journal will cover jumper changes to optimize the board for specific applications.

440 Alphabetics Construction (OSI 446)

The following instructions are for assembling the 440 board in conjunction with an OSI 400, an ASCII keyboard, and a video monitor or TV set (when used with a TV set, an ATV Research Pixie Verter or similar RF converter is necessary.).

Refer to the red/blue artwork and tissue overlay in conjunction with these instructions. ICs and IC sockets are specified by rows A through F indicated at the left of the board and a number counted from left to right. Example: the 2513 character generator is IC-B11.

Step 1.

Carefully inspect the 440 board for foil shorts and breaks. Cut any shorts with a sharp exacto knife or razor blade. The artwork shows a foil between Pin 10 and Pin 11 of IC F-1 (the 74123 at the lower left of the board). This foil should not be on the 440 board. If it is, cut it out.

Step 2. IC Installation

Install all ICs indicated on the parts overlay with the following exceptions:

A. Do not install any parts labeled G yet.

B. Do not install the 2102s or 2513 yet.

C. We strongly advise placing at least IC-F1 in a socket since it could be removed for a PC board option later.

Step 3. Resistors

Install the following vales at the specified locations:

R1	2.2K
R2	4.7K
R3	1K
R4	4.7K
R5	10K
R6, R7	1K
R8	220
R9	1K
R10	470
R11	220
R12, R13	1K
R14, R15	220
R16	1K
Pots	
R17	5K
R18	10K
R19	Jumper across its 3 pads (no pot)
R20	5K

Step 4. Capacitors

Install the following capacitors at the specified locations:

C1	6.8pf
C2	68pf (10 times C1)
C3	.1uf stable (ie. not bypass)
C4	.001uf
C5	25uf electrolytic (optional)
"C"	.1uf or larger bypass caps. 18 locations.

Step 5.

Install D1. Observe cathode orientation

Install a 16 pin socket at the keyboard connector.

Install four female Molex connectors along the right edge of the board.

Step 6. Jumpers

Install the address jumpers as shown at the lower right of the board. Install J1, J3, J5, J6, J7, J8, J12, and J13.

DO NOT INSTALL J2.

J4 will be installed later.

J9, J10, and J11 are for use with Pixie Verters only.

Step 7. Initial Testing

Apply +5 volts to the board and verify that power is present at all ICs. If a scope or frequency meter is available, perform the following tests:

1. Probing the pad near IC-F1 marked "clock in" with a Hi-Z probe, verify oscillator operation and adjust R17 for 4.000MHz operation. Verify operation of 74163 counter string.

2. Probing J1, adjust R18 for a period of 16.642 milliseconds.

3. An approximately 15,400Hz signal should be present at the pad marked J2.

4. Verify clock signals at the address pins of the 2102s and 2513 character generator.

5. If no test equipment is available, simply set R17 and R18 mid range and cross your fingers!

Step 8. Video Interfacing

1. Set R20 mid range

2. The following operations are to be done without 2102s or the 2513 present.

A. Video monitor connections. The Video "B" output is normally used to feed conventional closed circuit monitors. Best results are obtained when a Hi-Z termination is used. The monitor should be connected via an RF or phono jack using shielded cable.

B. TV set connections. Assemble the ATV Research Pixie Verter as per its instructions.

Then, install it on the 440 board such that its ground does not come into contact with the 440's ground. Set the Pixie Verter video drive pot mid range. Connect J9 to its + terminal, J10 to its minus terminal, and J11 to its video input (some sets will work better with J11 connected to video "B"). The pixie verter MUST be connected to the TV set via shielded cable!

Apply power to the 440 board and display. After adjusting vertical and horizontal hold circuits on your display, you should see about 28 vertical bars on underscanned monitors or about 24 vertical bars on a TV set. If the 440 was set up without test equipment, it will be necessary to adjust R17 to obtain this pattern. R18 should be used to adjust the frame rate for exactly 60Hz (so there is no power line interference) and to eliminate horizontal tearing across the top of the screen.

Step 9. Character Generator Installation

Install the 2513 character generator and apply +5 and -9 power. You should see a field of characters. By setting a six bit ASCII code on pins 17 through 22 of the 2513 via selective grounding and 1K pullups to +5,that corresponding ASCII code will appear on the entire screen.

Step 10. Memory Installation

Install six 2102 memories at IC-B2 through IC-B7. Power up the board--you should now observe random characters. At this time, adjust the contrast pot R20 for best picture. If a video monitor is used, picture quality should be as good as the best commercially available CRTs. If it is not, something may be mal-adjusted. If an RF link is used, picture quality will be much poorer.

Step 11. Keyboard Interfacing

A jumper, J4, is used to select negative or positive going keyboard flags. The jumper is configured in the parts layout diagram for negative flags. This jumper must be properly installed for OSI software compatibility. The connection table is given below for the SWTP keyboard and the Sanders 720 keyboard featured in Byte #1.

OSI 16 Pin Connector		SWTP	Sanders	
1	D_0	B	1	Both keyboards
2	D_1	C	2	have negative
3	D_2	D	3	going flags.
4	D_3	E	4	
5	D_4	F	5	
6	D_5	G	6	
7	D_6	H	7	
8	Ground	A	27 and 28	
9	Flag	J	21	
10				
11				
12				
13				
14				
15				
16	+5	K	26	

Step 12. Bringing Up a Video Based 400

If you have a 440 as the only I/O in the system, trouble shooting can be difficult because you are debugging the 400, 480, and 440 boards all at once. If there is any possibility of testing your 440 on someone else's system first, definately do so!

When using a 440 in conjunction with a 1K 400, the 400's memory must be decoded so that it does not occupy DXXX. This can be accomplished simply by the following:

1. Cut the tape to Pin 4 of IC-T (on the 400 board)
2. Jumper from B_{48} to Pins 1 and 2 of IC-T
3. Jumper from Pin 3 to Pin 4 of IC-T

This will partially decode the 2102s so they occupy 0000 through 7FFF.

When a V series system is properly operating, the TV screen is cleared on reset, leaving address 0000 and its contents on the screen. Any numeric key then typed on the screen will be displayed in the lower address character (000X). Consult the write-up accompanying your V series monitor for further details on operation. Refer to the trouble shooting table if any problems are encountered.

Step 13. 440 Board Use

A source listing for a CRT simulator routine is included. This routine or a modified version of it will allow you to use the 440 as a conventional CRT terminal.

Step 14. Options

A. Graphics

After you have become familiar with alphabetics, you may wish to expand to graphics.

1. Install all ICs labeled G

2. Install three sockets along the top of the board called GC1, GC2 , and GC3.

3. Populate a 420C board as per the graphics parts overlay with three sockets and 16 memories.

4. Remove J-13 and install a switch assembly in a convenient place as per diagram G-1.

5. Connect the graphics memory to the 440 via three SHORT 16 pin ribbon cables. Refer to the OSI Systems Journal for graphics based programs.

6. It is desirable to blank graphics during the initial dialog with a V series PROM monitor since the random garbage in the graphics memory would mask the alphabetics display. Graphics should also be blanked during graphics memory transfers at animation rates to eliminate noise in the picture.

B. Crystal Controlled Clock

The 440 is set up to be run from a master clock instead of the 74123 clock. A 4MHz crystal control signal can be obtained from the 470 or upcoming OSI CPU boards. However, a simple 4.000 MHz crystal clock can be installed directly above the existing 74123 clock as per diagram G2.

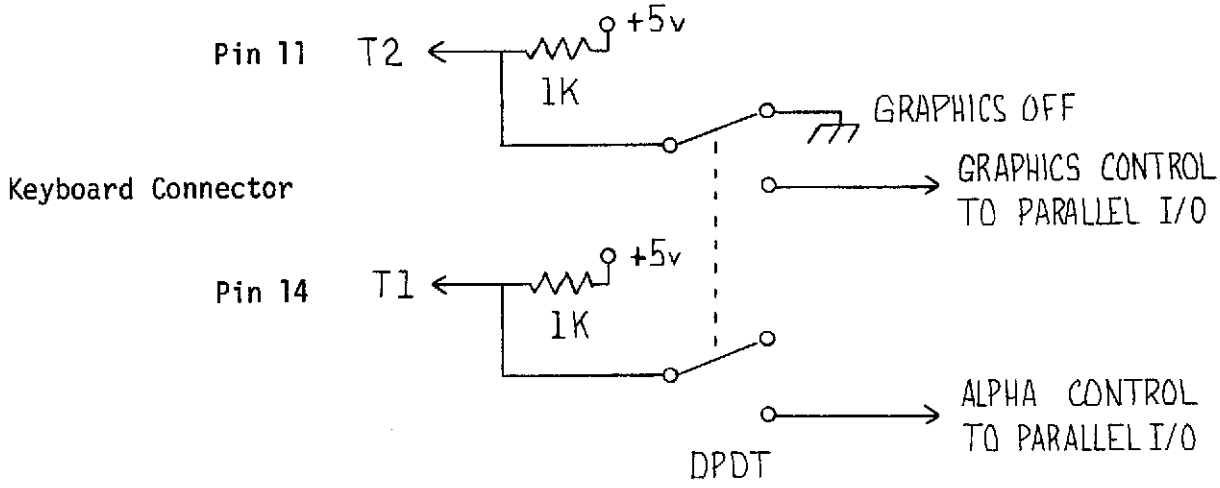
C. Color

A simple four color modification can be made for direct gun connection to a color monitor. Direct connection provides

stable saturated high resolution color, unlike the video approach of the "other" video board with color.

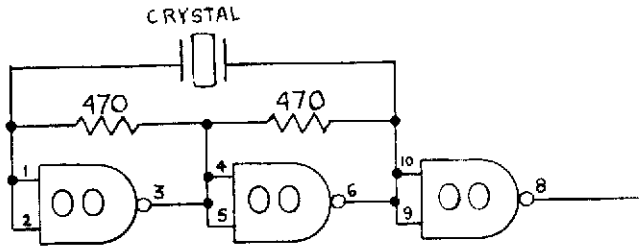
To implement color, install the two optional 2102s and implement the circuit shown in diagram G3 on a prototyping board or the prototyping area of the Video Graphics board. The 15 volt open collectors should easily interface to most modern color sets gun drivers. However, observe our previous warnings about TV isolation.

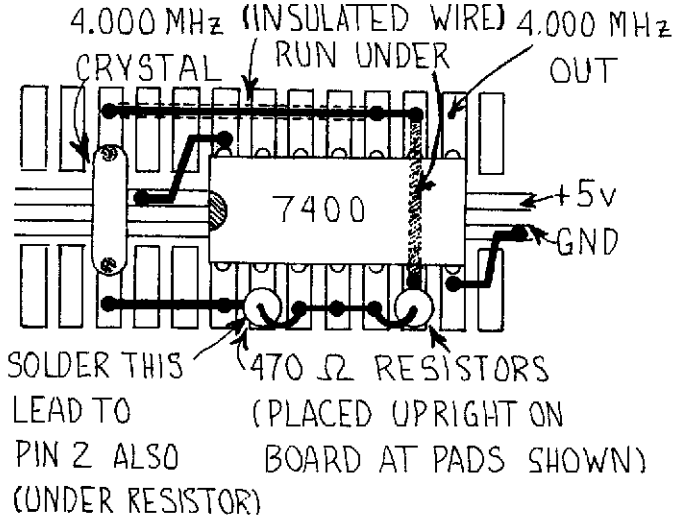
USER INSTALLED EXTERNAL SWITCH FOR GRAPHICS OPTION



Ground is available at Pin 8

+5 is available at Pin 16

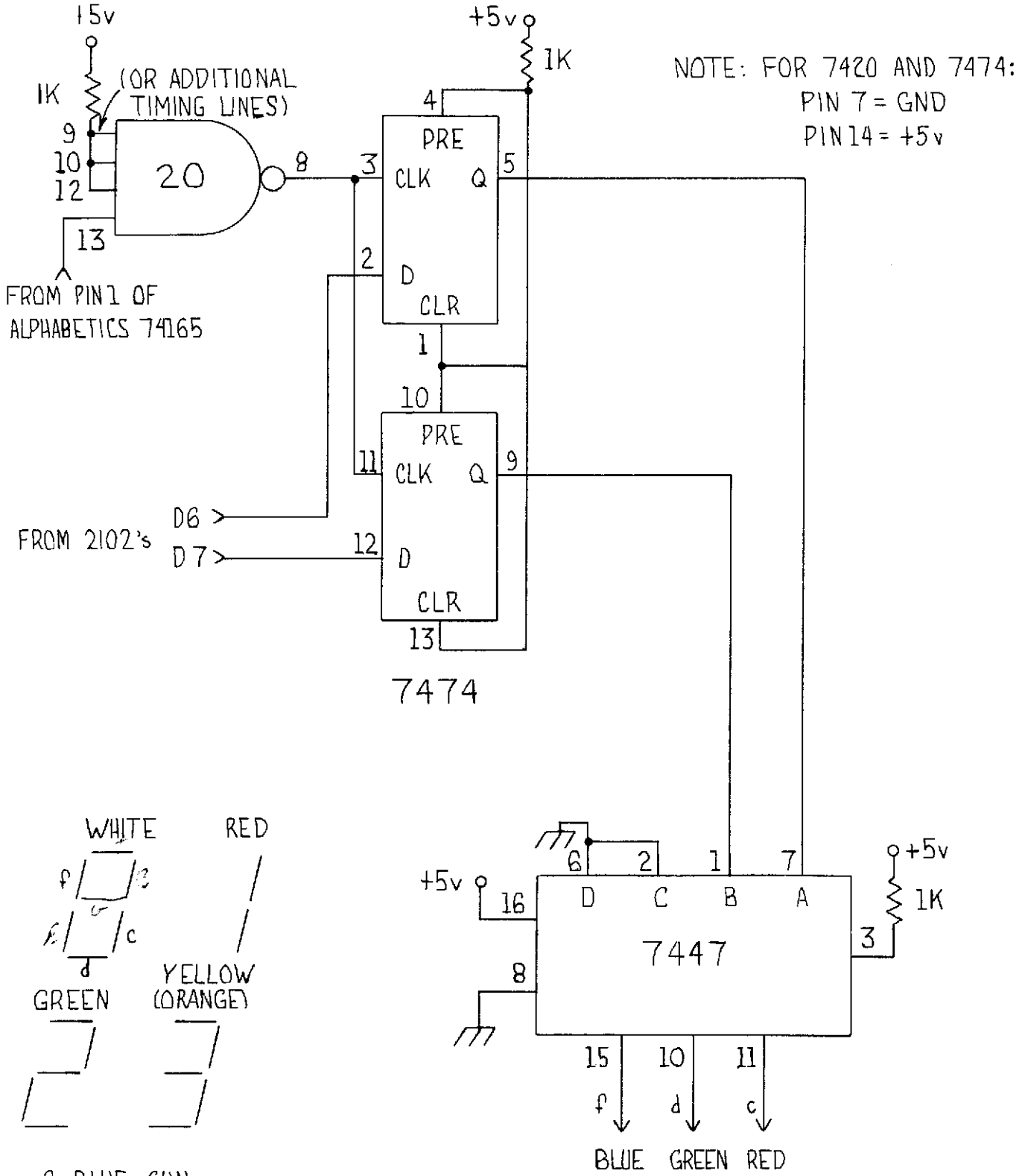




• DENOTES SOLDER JOINT

440 CRYSTAL CLOCK MODIFICATION

G-2



COLOR IMPLEMENTATION

Trouble Shooting

A. Can't get down to 4.000MHz with R17: PLACE A 10K RESISTOR IN PARALLEL WITH R2.

B. Clock Stops Occasionally: FAULTY 74123 IC-F1

System Power Up Problems:

C. Nothing happens on reset: CHECK DATA LINES FROM THE EDGE CONNECTOR TO THE 8T26s D1, THE ADDRESS JUMPERS, AND THE SYSTEM ADDRESS LINES TO THE 74157s FOR SHORTS WHICH MIGHT HANG UP THE SYSTEM.

D. Screen does not reset to blanks: THE PROCESSOR LOADS (20) HEX INTO EACH LOCATION. IF A MEMORY IS BAD OR A DATA LINE SHORT EXISTS ON THE BOARD, SOME OTHER CHARACTER (OTHER THAN SPACE) WILL BE GENERATED.

E. On reset, the screen is predominantly blank but more than six characters are present: BAD MEMORY OR MEMORY ADDRESS LINE OPEN OR SHORT.

F. Screen resets fine but will not acknowledge keyboard: CHECK 74125 CIRCUITRY. CHECK KEYBOARD'S STROBE PULSE; IT SHOULD BE AT LEAST 50USEC. LONG TO WORK.

G. Keystroke is not acknowledged until the next key is depressed: J4 IS IMPROPERLY INSTALLED.

Operational Problems:

H. Snow or noise in picture at all times: POWER SUPPLY DECOUPLING INADEQUATE OR BAD CHARACTER GENERATOR OR FAULTY 7408 AT IC-A4 OR A5.

I. Noise in picture only when processor is present: POWER SUPPLY DECOUPLING OR GROUND PROBLEM.

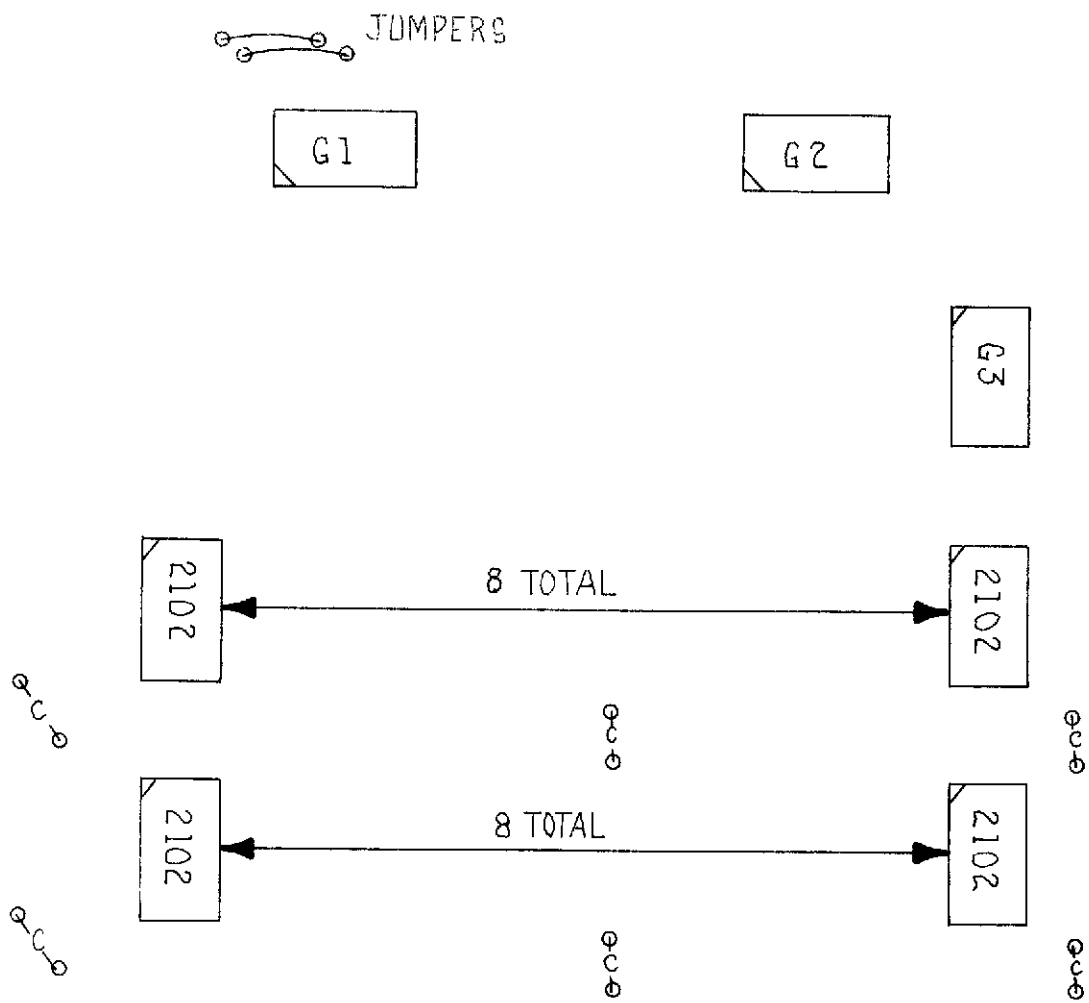
J. Noise in picture only when keyboard is present: NOISE PICK-UP ON KEYBOARD CABLE MAY BE ELIMINATED BY SETTING A "20" ON THE CHARACTER GENERATOR INPUTS; PIN 17 THROUGH 22 WITH 10K RESISTORS TO +5 AND GROUND (22 TO +5 OTHERS TO GROUND).

K. Keyboard works with 65V and some programs but not others such as "graphics editor" or extended monitor: J4 IMPROPERLY INSTALLED OR KEYBOARD STROBE TOO SHORT.

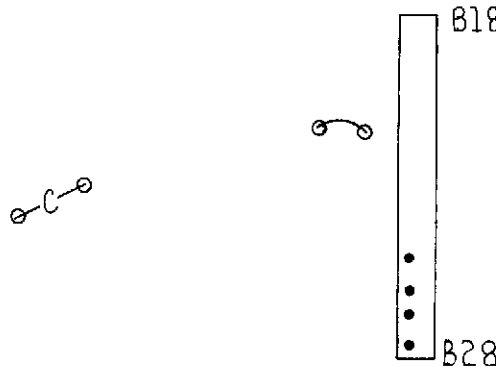
L. Characters change, are wrong, or mysteriously appear on the screen: DISPLAY MEMORY IS NOT ZERO DATA HOLD TYPE MEMORY OR MEMORY ACCESS TIME IS TOO SLOW FOR SYSTEM CLOCK SPEED OR MEMORY IS FAULTY.

M. Keyboard noise appeared when graphics was installed: A "SLOW POLL" ROUTINE MUST BE USED WHEN GRAPHICS IS ENABLED OR KEYBOARD POLLING WILL MASK THE SCREEN. IF NOISE EXISTS WITH GRAPHICS DISABLED, GO TO SYMPTOM J.

N. Symptom L. appeared only after graphics was installed: EXTRA BUFFERING REQUIRED ON R/W TO THE GRAPHICS MEMORY. INSERT TWO 7404 TYPE INVERTERS IN THE SIGNAL LINE FROM THE MULTIPLEXER TO PIN 3 OF GC3 (IC-A3).

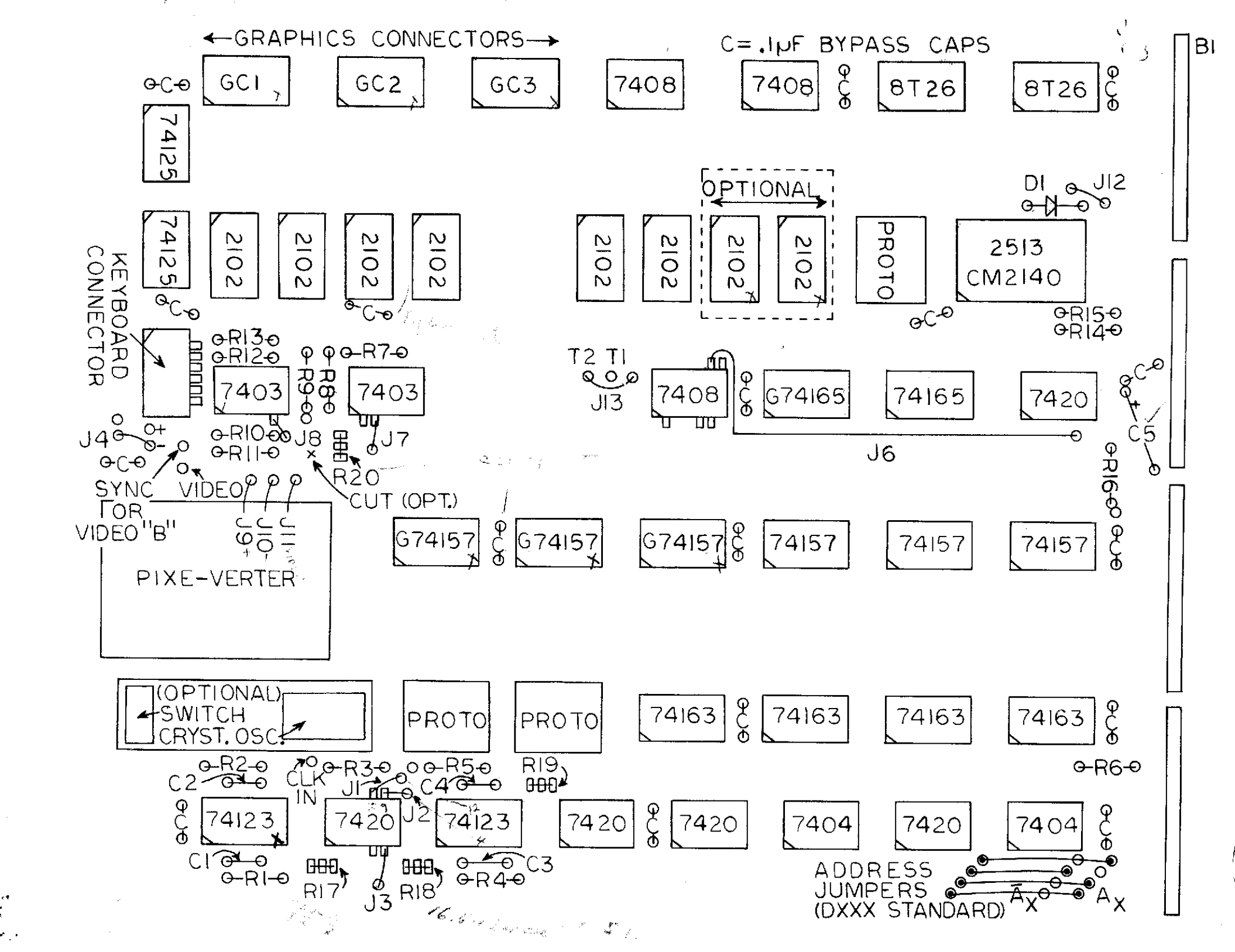


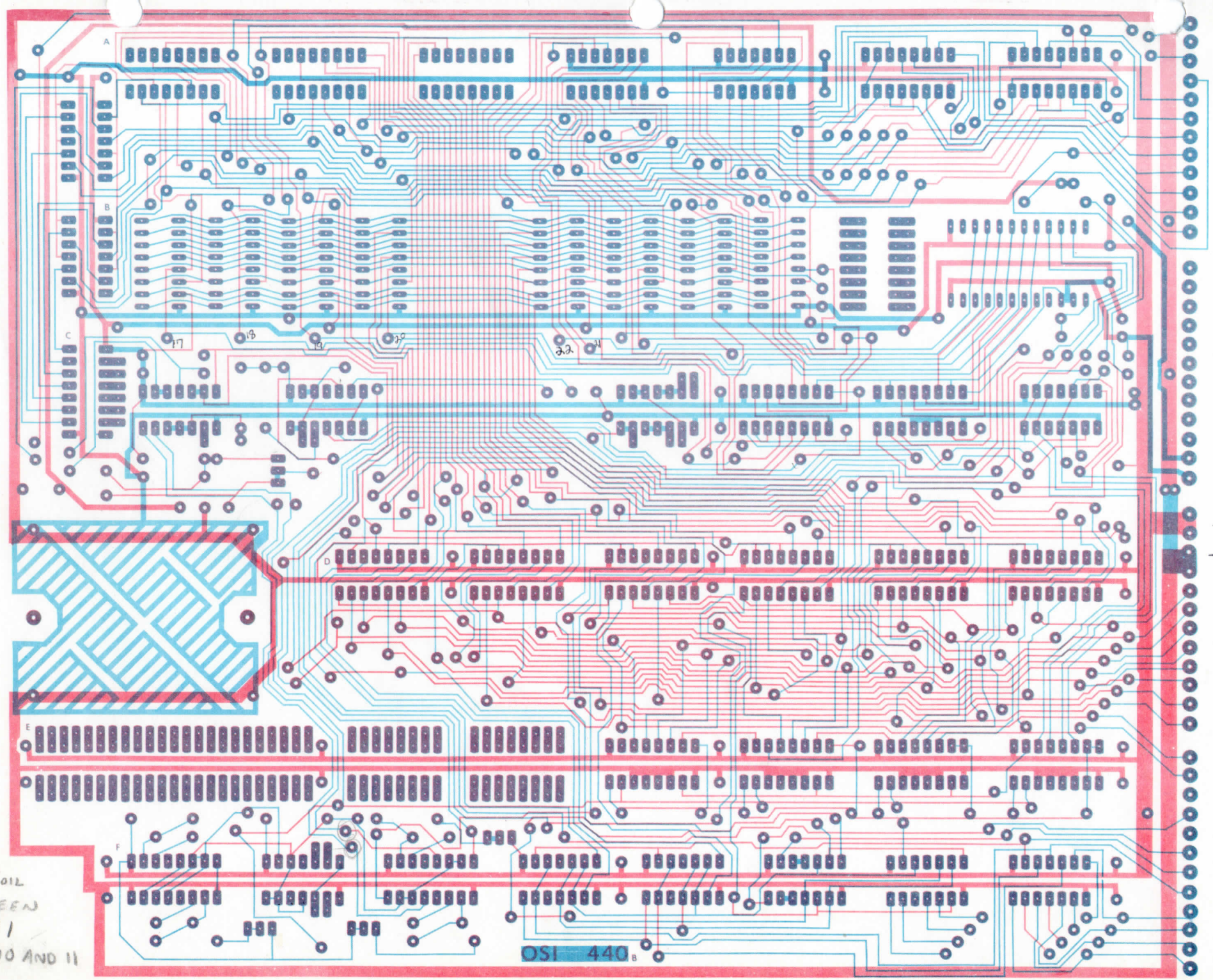
C=.1μf BYPASS CAPACITORS



NOTE: POSITION MOLEX WITH LOWEST PIN IN B28. DO NOT CONNECT TO ADDRESS LINES (B29 – B36)! POWER CONNECTION ONLY!

420C GRAPHICS MEMORY OVERLAY


←GRAPHICS CONNECTORS→
C=.1μF BYPASS CAPS
B1
GC1
GC2
GC3
7408
7408
8T26
8T26
74125
74125
2102
2102
2102
2102
2102
2102
2102
2102
OPTIONAL
PROTO
D1
J12
2513
CM2140
R15
R14
KEYBOARD CONNECTOR
R13
R12
R9
R6
R7
7403
7403
T2 T1
J13
7408
G74165
74165
7420
C5
J4
R10
R11
J8
J7
R20
J6
R16
SYNC
VIDEO
OR VIDEO "B"
CUT (OPT.)
J9
J10
J11
PIXE-VERTER
G74157
G74157
G74157
74157
74157
74157
(OPTIONAL) SWITCH CRYST. OSC.
PROTO
PROTO
74163
74163
74163
74163
R6
R2
R3
R5
R19
C2
CLK IN
J1
C4
74123
7420
J2
74123
7420
7420
7404
7420
7404
C1
R1
R17
J3
R18
R4
C3
ADDRESS JUMPERS (DXXX STANDARD)
$\bar{A}_X$
A_X



CUT FOIL
BETWEEN
IC-F1
PIN 10 AND 11