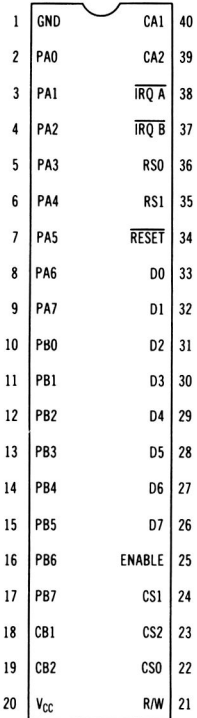


# 510 REV. C BOARD PINOUTS

S6821P



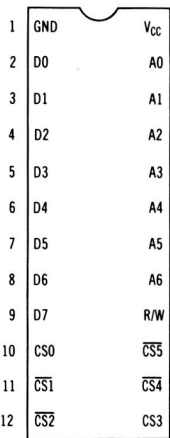
U1

MC6850P



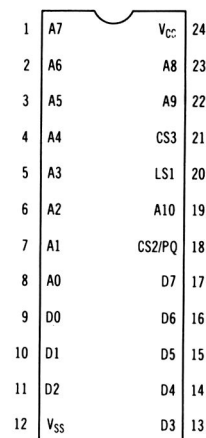
U2

MCM68B10P



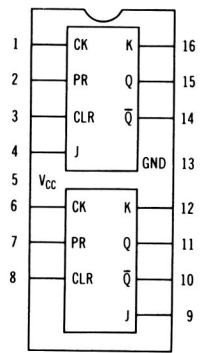
U3

2716/2316B



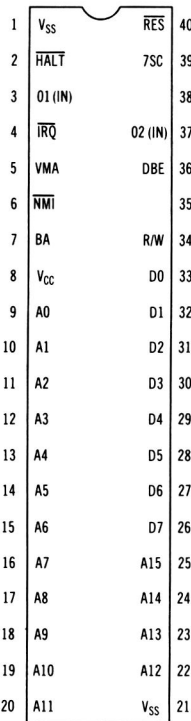
U4,U46

DM7476N



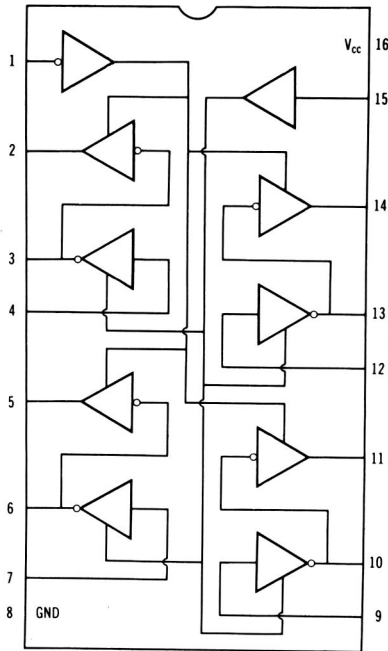
U5

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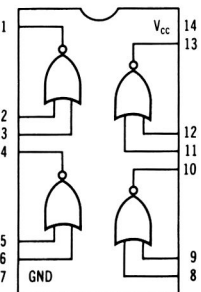
U7

N8T26N



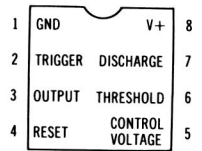
U8,U9,U10,U11,U29,U30,U48,U49

SN7420N



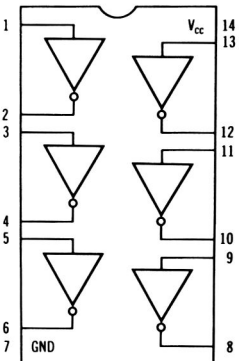
U6

555



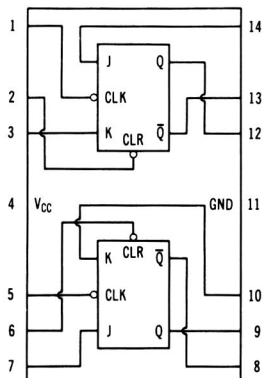
U12

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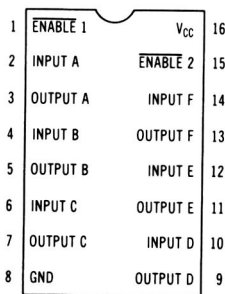
U13,U19,U33,U36,  
U43,U52,U54

SN7473N



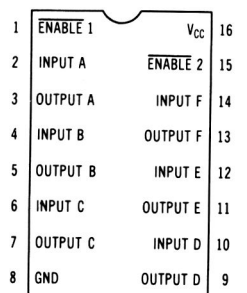
U14

MC8T95P



U15,U17,U18,U20,U26,U27,  
U39,U40,U55,U56,U57,U58

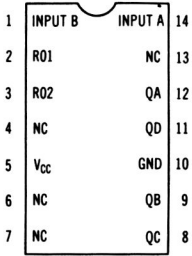
N8T95N



U16

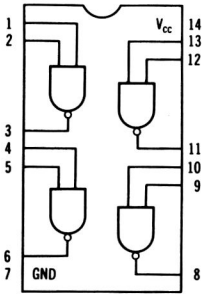
# 510 REV. C BOARD PINOUTS (CONTINUED)

SN7493AN



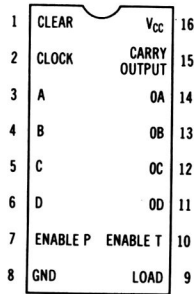
U21,U22

SN7400N



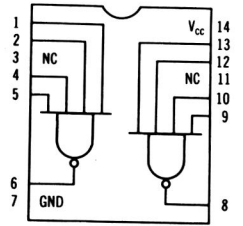
U23,U31,U34,U44,U53

74163N



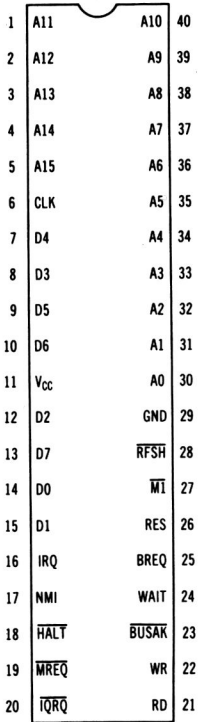
U24

SN7420N



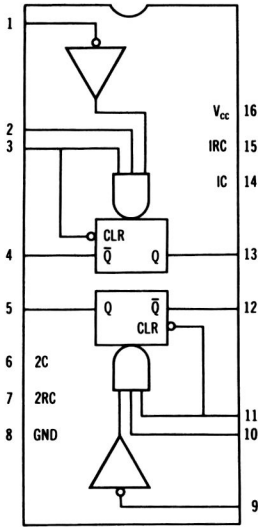
U25

Z-80



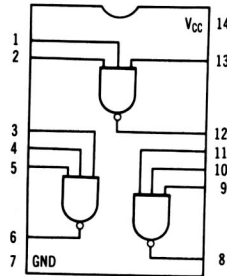
U28

74123N



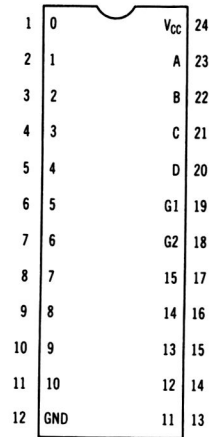
U32

F5410DM



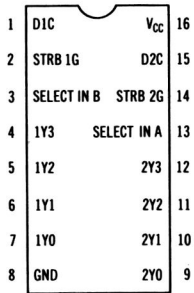
U34,U37

SN74154N



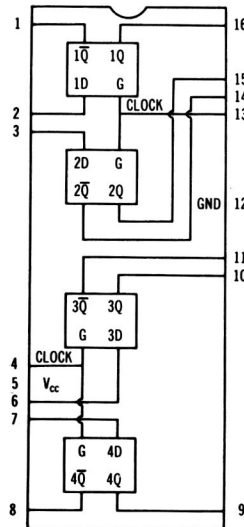
U38

F74155PC



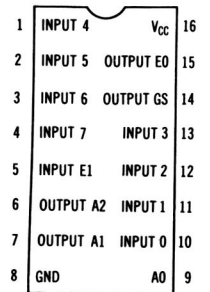
U41

DM7475N

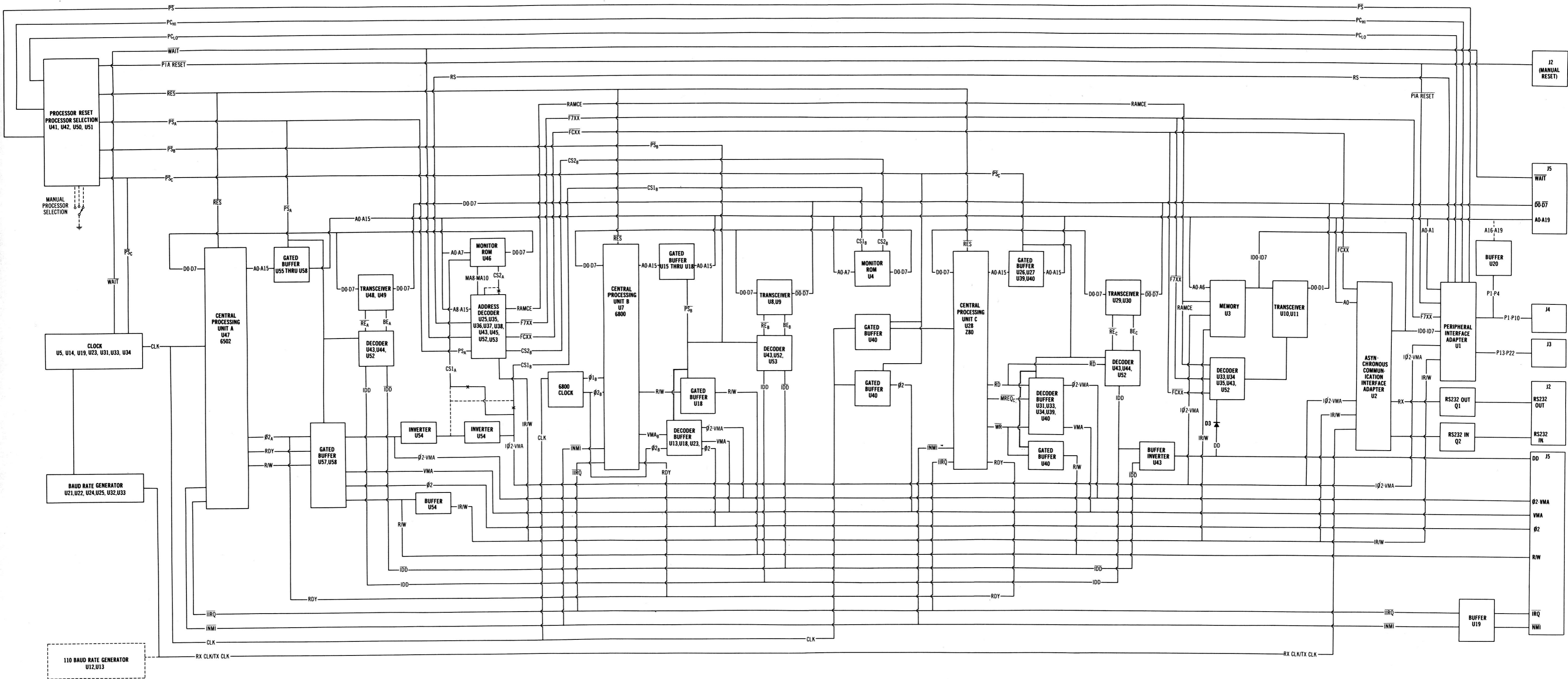


U42

74148N



U45



510 REV. C BOARD BLOCK

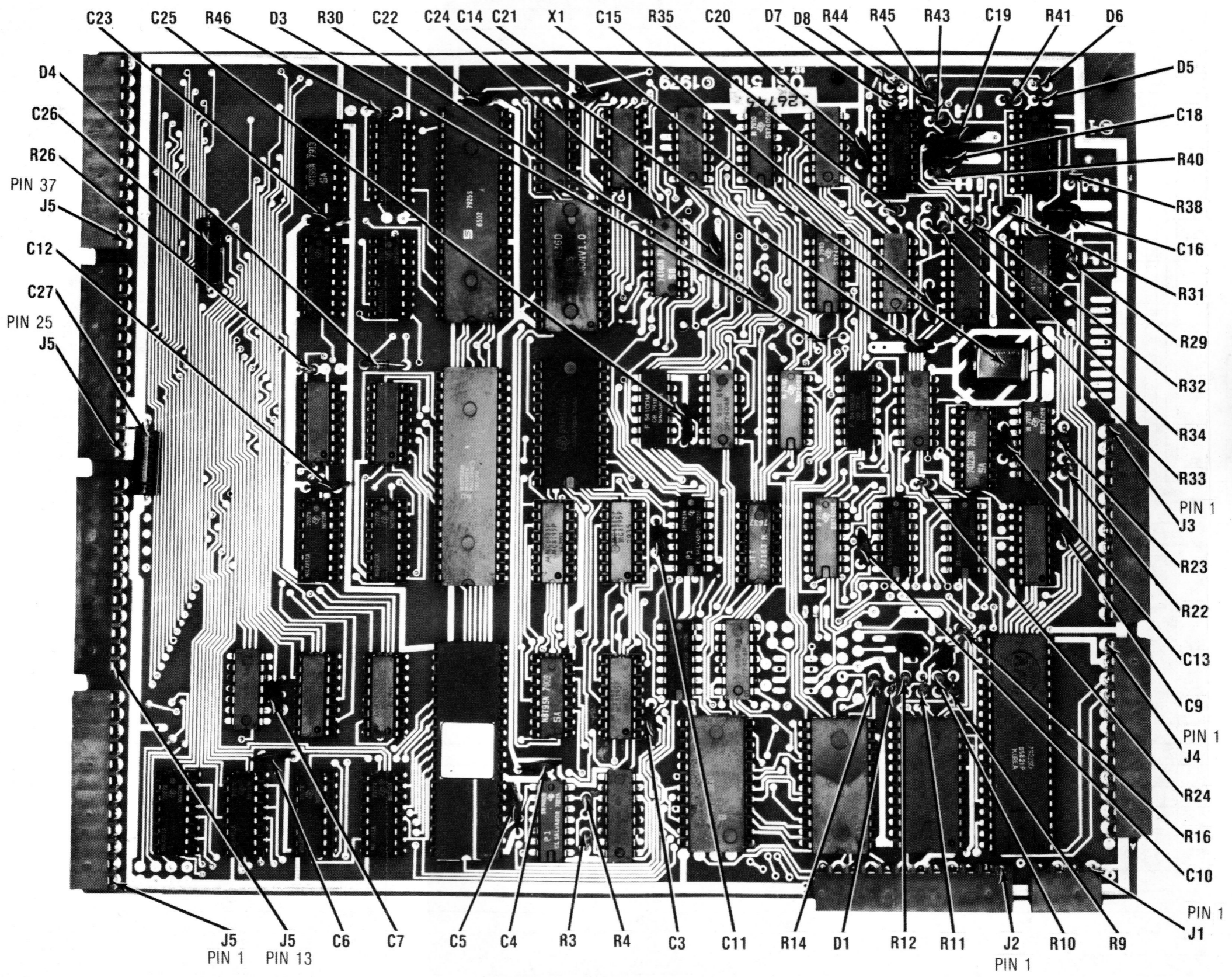
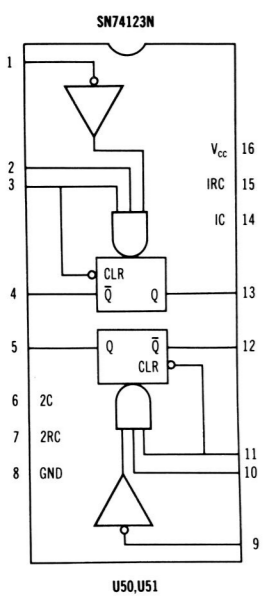
510 REV. C BOARD BLOCK

# 510 REV. C BOARD PINOUTS (CONTINUED)

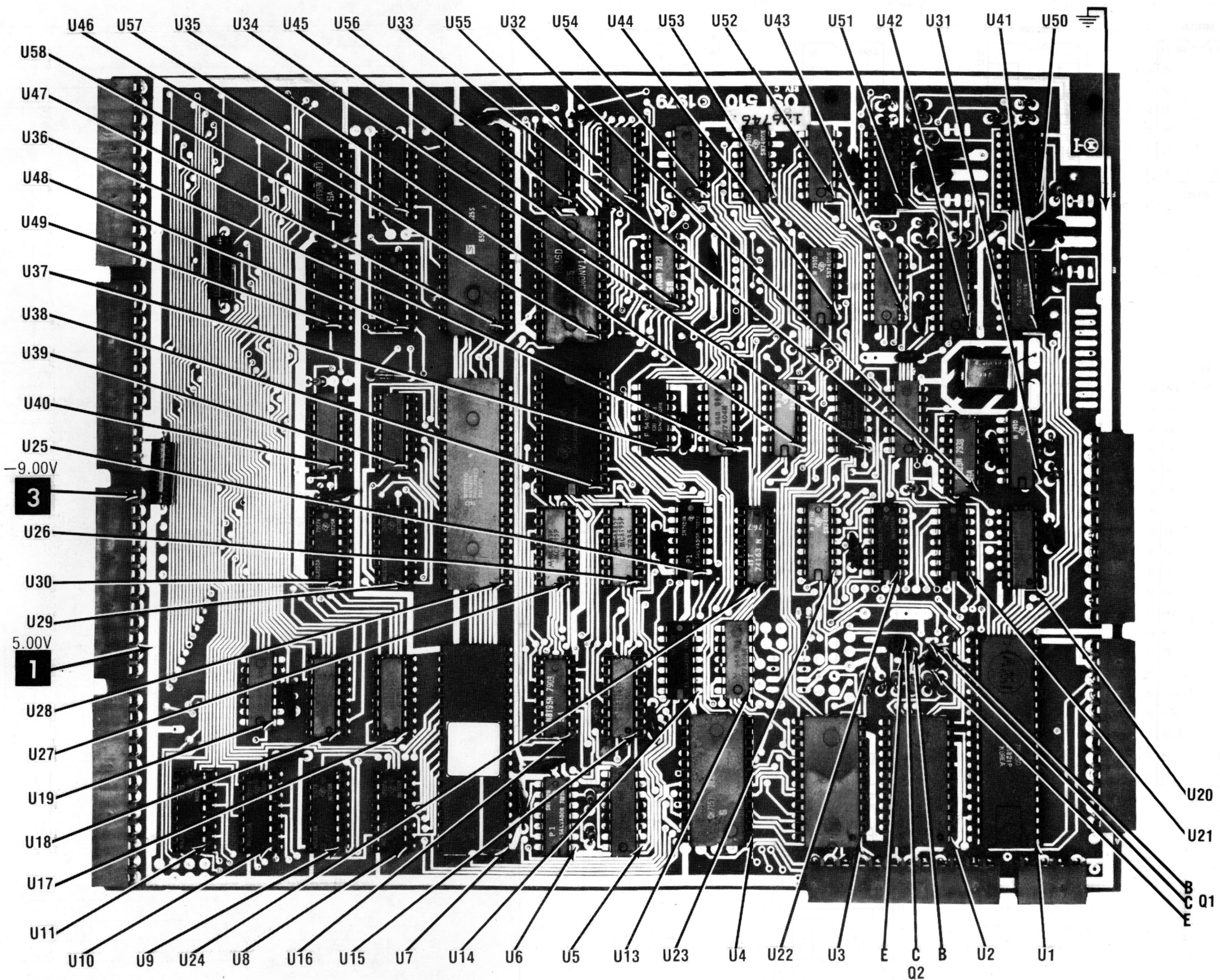
6502

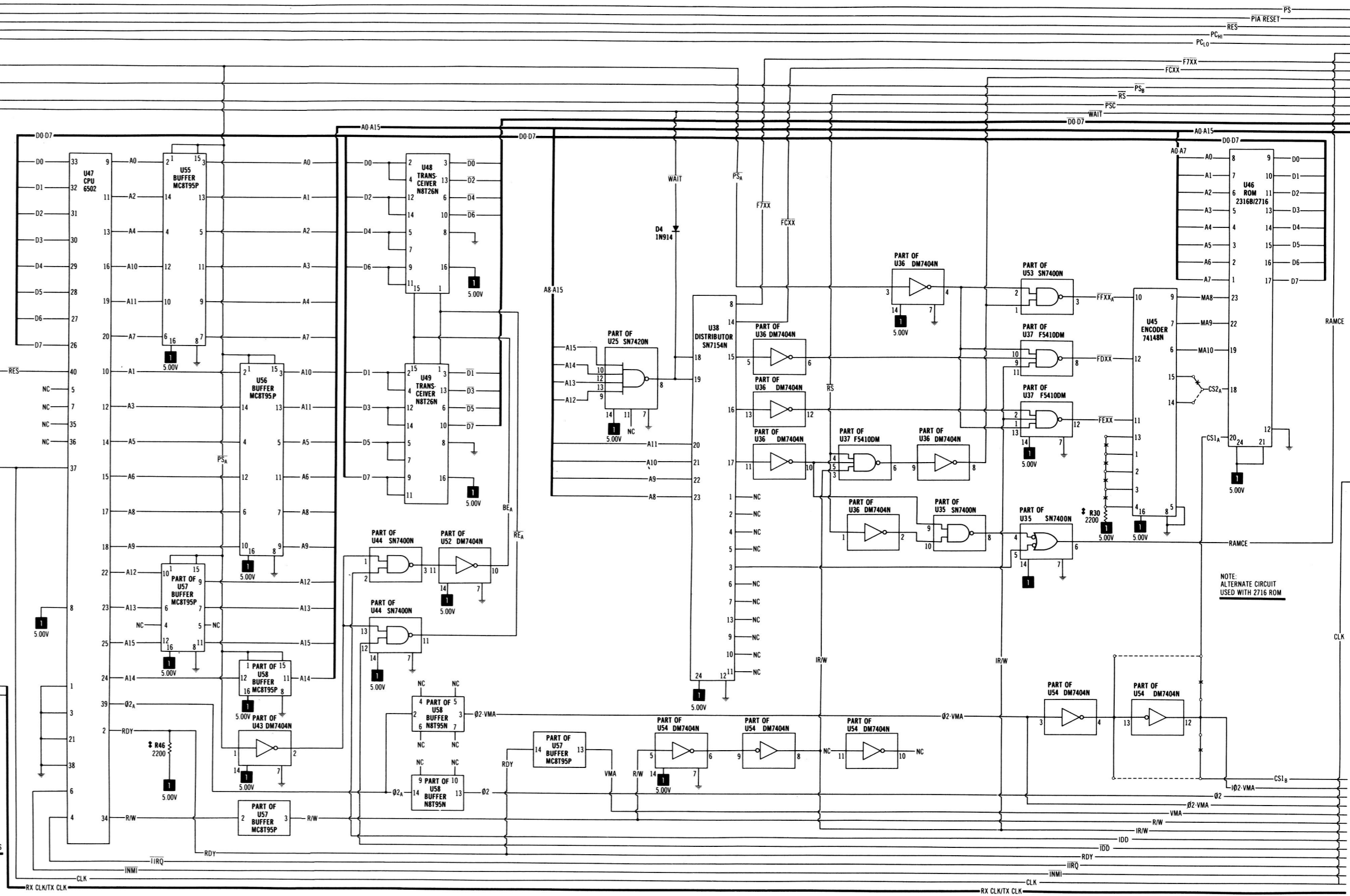
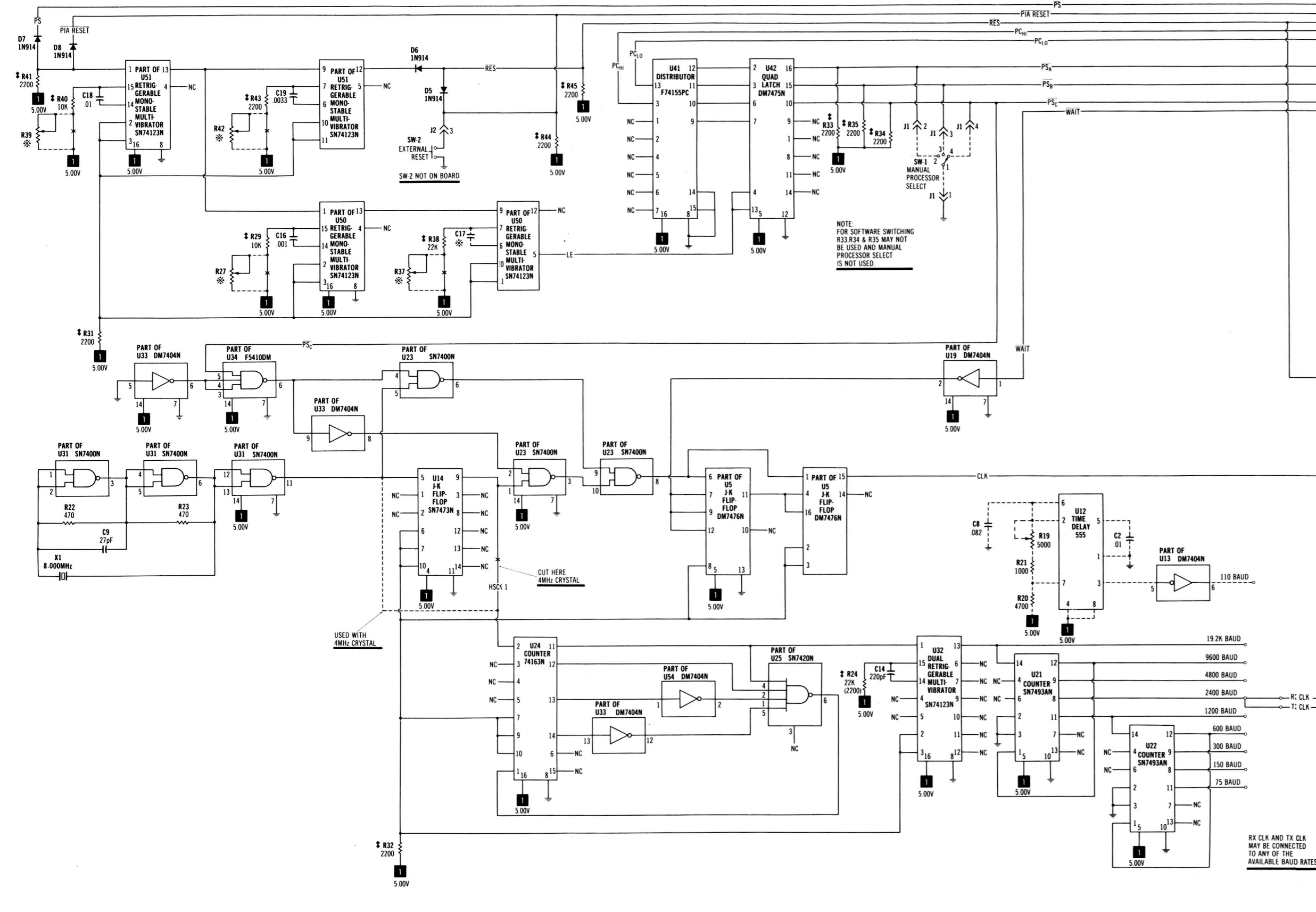
1	VSS	RES	40
2	RDY	Ø2 (OUT)	39
3	Ø1 (OUT)	S.O.	38
4	IRQ	Ø0(IN)	37
5	N.C.	N.C.	36
6	NMI	N.C.	35
7	SYNC	R/W	34
8	VCC	DB0	33
9	AB0	DB1	32
10	AB1	DB2	31
11	AB2	DB3	30
12	AB3	DB4	29
13	AB4	DB5	28
14	AB5	DB6	27
15	AB6	DB7	26
16	AB7	AB15	25
17	AB8	AB14	24
18	AB9	AB13	23
19	AB10	AB12	22
20	AB11	VSS	21

U47

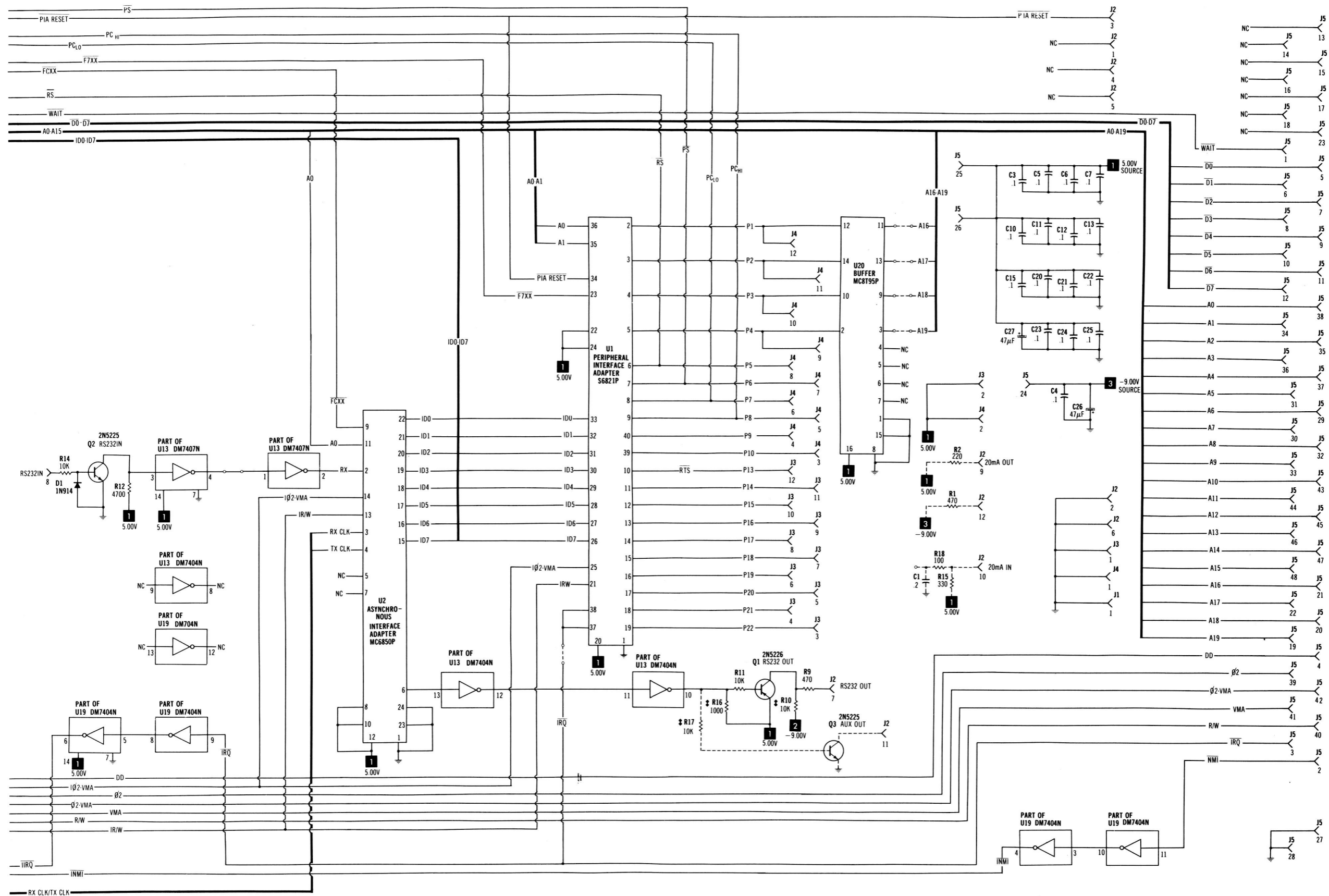


## 510 REV. C BOARD











**505 BOARD  
(CONTINUED)**

**510 BOARD  
(CONTINUED)**

NMI.....Non-Maskable Interrupt  
 PA0-PA7.....Port A  
 PB0-PB7.....Port B  
 READY DRIVE 1.....Ready Drive One  
 READY DRIVE 2.....Ready Drive Two  
 RES.....Reset  
 R/W.....Read/Write  
 SECTOR.....Sector  
 SELECT DRIVE 1.....Select Drive One  
 SELECT DRIVE 2.....Select Drive Two  
 SEP DATA.....Separated Data  
 SEP CLOCK.....Separated Clock  
 STEP.....Step  
 STEP IN.....Step In  
 TRACK 00.....Track Zero  
 TX CLK.....Transmit Clock  
 VMA.....Valid Memory Address  
 WRITE DATA.....Write Data  
 WRITE ENABLE.....Write Enable  
 WRITE PROTECT.....Write Protect  
 Ø0.....Phase Zero  
 Ø2.....Phase Two  
 Ø2·VMA.....Phase Two·Valid  
 Memory Address

DD.....Data Direct  
 F7XX.....Address F7XX<sub>16</sub>  
 FCXX.....Address FCXX<sub>16</sub>  
 FDXX.....Address FDXX<sub>16</sub>  
 FEXX.....Address FEXX<sub>16</sub>  
 FFX<sub>A</sub>.....Address FFX(6502)  
 FFX<sub>B</sub>.....Address FFX(6800)  
 HSCK1.....High Speed Clock One  
 HIS.....High Speed  
 ID0-ID7.....Internal Data  
 IDD.....Internal Data Direct  
 IIRQ.....Internal Interrupt Request  
 INMI.....Internal Non-maskable Interrupt  
 IRQ.....Interrupt Request  
 IR/W.....Internal Read/Write  
 IØ2·VMA.....Internal Phase Two·Valid  
 Memory Address  
 MA8-MA10.....Memory Address  
 MREQ<sub>C</sub>.....Memory Request  
 NMI.....Non-maskable Interrupt  
 P1-P22.....Port  
 PC<sub>H1</sub>.....Processor Select High  
 PC<sub>LO</sub>.....Processor Select Low  
 PIA RESET.....Peripheral Interface  
 Adapter Reset  
 PS.....Processor Select  
 PS<sub>A</sub>.....6502 Select  
 PS<sub>B</sub>.....6800 Select  
 PS<sub>C</sub>.....Z-80 Select  
 RAMCE.....Random Access Memory  
 Chip Enable  
 RD.....Z80 Read  
 RDY.....Ready  
 RE<sub>A</sub>.....Read Enable(6502)  
 RE<sub>B</sub>.....Read Enable(6800)  
 RES.....Reset  
 RFSH<sub>C</sub>.....Refresh  
 RS.....Ram Select  
 R/W.....Read/Write

**LEGEND FOR 510 REV. C  
BOARD SCHEMATIC**

A0-A19.....Address  
 BØ2.....Buffer Phase Two  
 BE<sub>A</sub>.....Bus Enable (Processor 6502)  
 BE<sub>B</sub>.....Bus Enable (Processor 6800)  
 CLK.....Clock  
 CS1<sub>A</sub>.....6502 Rom Chip Select  
 CS1<sub>B</sub>.....6800 Rom Chip Select  
 CS2<sub>A</sub>.....6502 Rom Chip Select  
 CS2<sub>B</sub>.....6800 Rom Chip Select  
 D0-D7.....Data

Any  $\overline{\text{Bar}}$  above any alphabetical or numerical combination indicates line active in a low (0) state.

