560Z CPU Expander Board

Description:

The 560Z CPU Expander is a "computer lab on a board." The 560Z supports Z-80 (8080 up-grade) and IM-6100 (PDP-8 compatible) microprocessors plus three-way bus switches and run/single step circuitry. The 560Z runs under the command of a 6502-based Ohio Scientific 400, 500, or 510 System.

Applications:

The 560Z can run standard PDP-8 and 8080 programs on an Ohio Scientific computer. It also has tremendous value as an educational aid in teaching about microprocessors since the host 6502 can single step the other two processors and read the status of each of their signal lines! The 560Z is a powerful research tool for investigations in multiprocessing and other computer architecture. The 560Z has provisions for a third microprocessor so new microprocessors can be evaluated under a complete operating system soon after their introduction.
Note: The 560Z is not for beginners. It is recommended that the potential 560Z user become intimately familiar with the 6502 system before attempting to utilize the 560Z.

Specifications:

Mechanical: 8" X 10" G-10 Double-Sided Plated Through Hole Board. 48-Pin System Bus on One Edge, 48 Pin Sub-Bus on Other Edge.

Electrical: +5V at 600ma

Supports: Z-80 and/or 6100 Microprocessors Plus Provisions for a Third Processor.

Hardware Requirements: System Bus Side: 400, 500 or 510 CPU with 6502 Processor and at Least 4K X 8 RAM
Sub Bus Side: 4K X 8 RAM for Z-80 Only, 4K X 12 RAM for 6100 Only or 6100 and Z-80

Mounting: The 560Z's Sub-Bus can support a full 65K of memory and I/O, but, it only occupies 4,512 bytes of the 6502 memory space via a sliding "port-hole." A 560Z and one dedicated memory can be mounted in slot 1 of the Challenger. If additional memory is required, an additional case will be required.

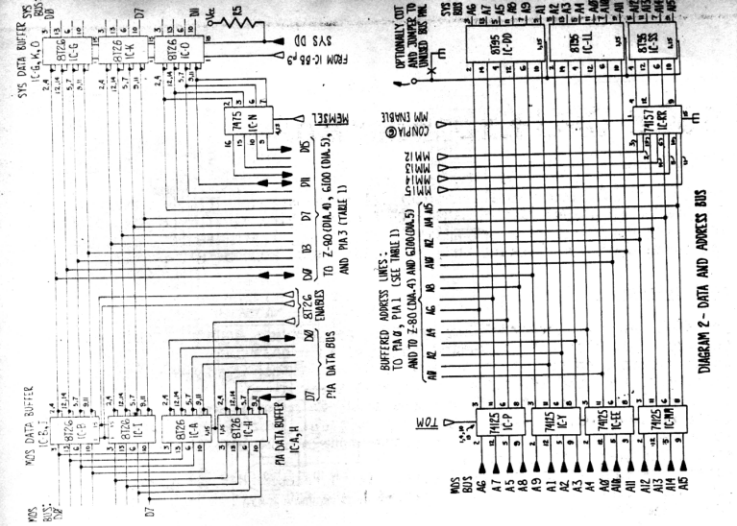


DIAGRAM 2 - DATA AND ADDRESS BUS

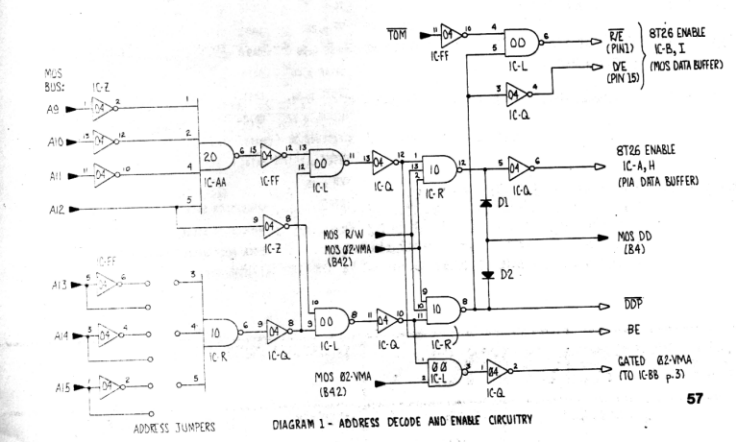


DIAGRAM 1 - ADDRESS DECODE AND ENABLE CIRCUITRY

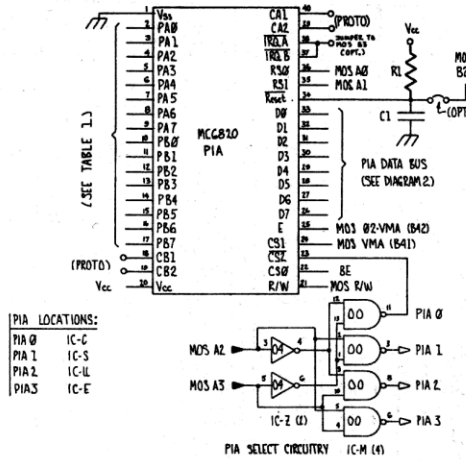


DIAGRAM 3 - PIA IMPLEMENTATION

	PIAØ IC-C	PIA1 IC-S	PIA2 IC-U	PIA3 IC-E
PAØ	AØ	A8	$\overline{WR}$ p.22	DA8
PA1	A1	A9	$\overline{MREQ}$ p.19	DA9
PA2	A2	A10	DATAF p.40	DA1Ø
PA3	A3	A11	$\overline{CFSEL}$ p.38	DA11
PA4	A4	A12	$\overline{MEMSEL}$ p.37	DA12
PA5	A5	A13	IFETCH p.36	DA13
PA6	A6	A14	$\overline{RESET}$ p.7	DA14
PA7	A7	A15	$\overline{SKP}$ p.35	DA15
PBØ	Z-80 $\overline{RFSH}$ p.10	DØ	$\overline{INTREQ}$	*PROCESSOR SELECT
PB1	Z-80 $\overline{INT}$ p.11	D1	$\overline{\Phi}_2$	*PROCESSOR SELECT
PB2	Z-80 $\overline{IORQ}$ p.12	D2	$\overline{\Phi}_1$	CLOCK MODE SELECT (RUN/STEP)
PB3	MM STROBE	D3	$\overline{\Phi}_0$	6100 $\overline{RUN/HALT}$
PB4	MM12	D4	LXMAR	STEP
PB5	MM13	D5	$\overline{SWSEL}$	$\overline{W}_1$ p.27
PB6	MM14	D6	XTC	$\overline{RESET}$ p.26
PB7	MM15	D7	$\overline{DEVSEL}$	$\overline{BUSAK}$ p.28

*See Selection Table, Diagram 6.

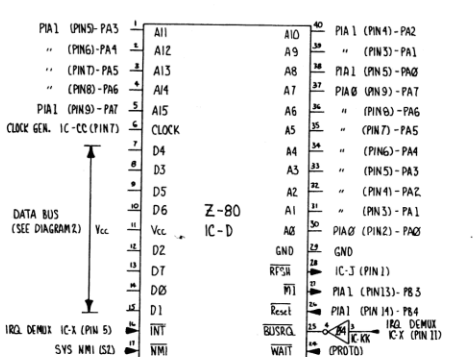
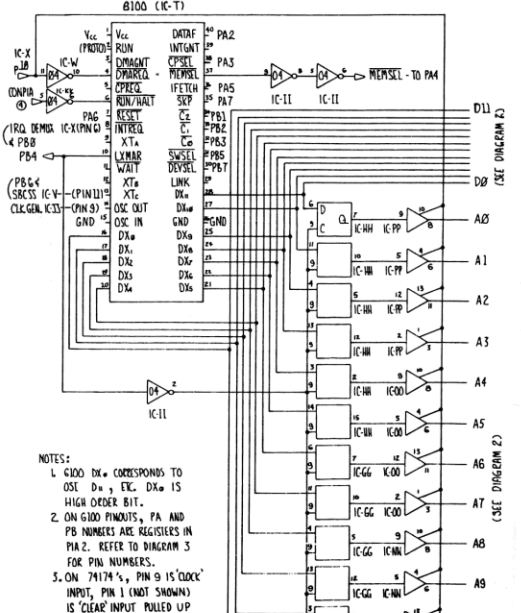


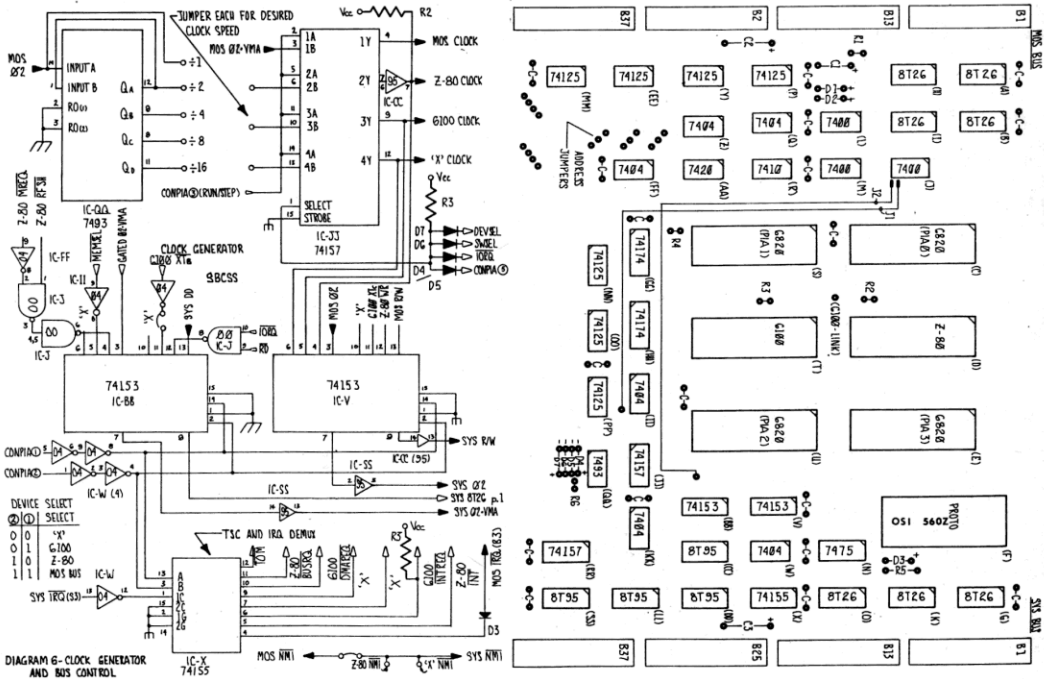
DIAGRAM 4 - Z-80 PINOUTS



NOTES:

1. G100 DX∎ CORRESPONDS TO OSE D∎ ; ETC. DX∎ IS HIGH ORDER BIT.
2. ON G100 PINOUTS, PA AND PB NUMBERS ARE REGISTERS IN PIA 2. REFER TO DIAGRAM 3 FOR PIN NUMBERS.
3. ON 74174's, PIN 9 IS 'CLOCK' INPUT, PIN 1 (NOT SHOWN) IS 'CLEAR' INPUT PULLED UP THROUGH 1K RESISTOR.
4. IC-GG, HH - 74174. IC-NN, OO, PP - 74175

DIAGRAM 5 - G100 PINOUTS AND ADDRESS LATCH


JUMPER EACH FOR DESIRED CLOCK SPEED
MOS ØZ-YMA
MOS Ø2
INPUT A
INPUT B
÷1
÷2
÷4
÷8
÷16
IC-QQ 7493
CONPIA (RUN/STEP)
SELECT STROBE
IC-JJ 74157
Vcc
R2
R3
1A 1B 1Y
2A 2B 2Y
3A 3B 3Y
4A 4B 4Y
MOS CLOCK
Z-80 CLOCK
6100 CLOCK
'X' CLOCK
IC-CC
D7 DEVSEL
D6 SWSEL
IORQ
D4 CONPIA
D5
MOS RESET
Z-80 RESET
CLOCK GENERATOR
8BCSS
IC-FF
IC-II
IC-3
IC-J
GATED WAIT
SYS 00
IORQ
RD
WR
74153 IC-BB
74153 IC-V
SYS R/W
IC-SS
SYS ØZ
SYS ØZ20 p1
SYS ØZ-YMA
CONPIAD
CONPIAC
IC-W (4)
DEVICE SELECT
SELECT
'X'
6100
Z-80
MOS BUS
TSC AND IRQ DEMUX
IC-X 74155
R5
D3
SYS IRQ (83)
MOS IRQ (83)
MOS NMI
Z-80 NMI
'X' NMI
SYS NMI
DIAGRAM 6- CLOCK GENERATOR AND BUS CONTROL
MOS BUS
SYS BUS
ADDRESS JUMPERS
74125
74174
74153
74157
74155
74175
74LS93
8T26
8T95
7404
7408
7410
7420
C828 (PIA1)
C828 (PIA2)
C100
Z-80
C100-INTX
6820 (PIA2)
6820 (PIA3)
PROTO OSI 560Z
J1
J2
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