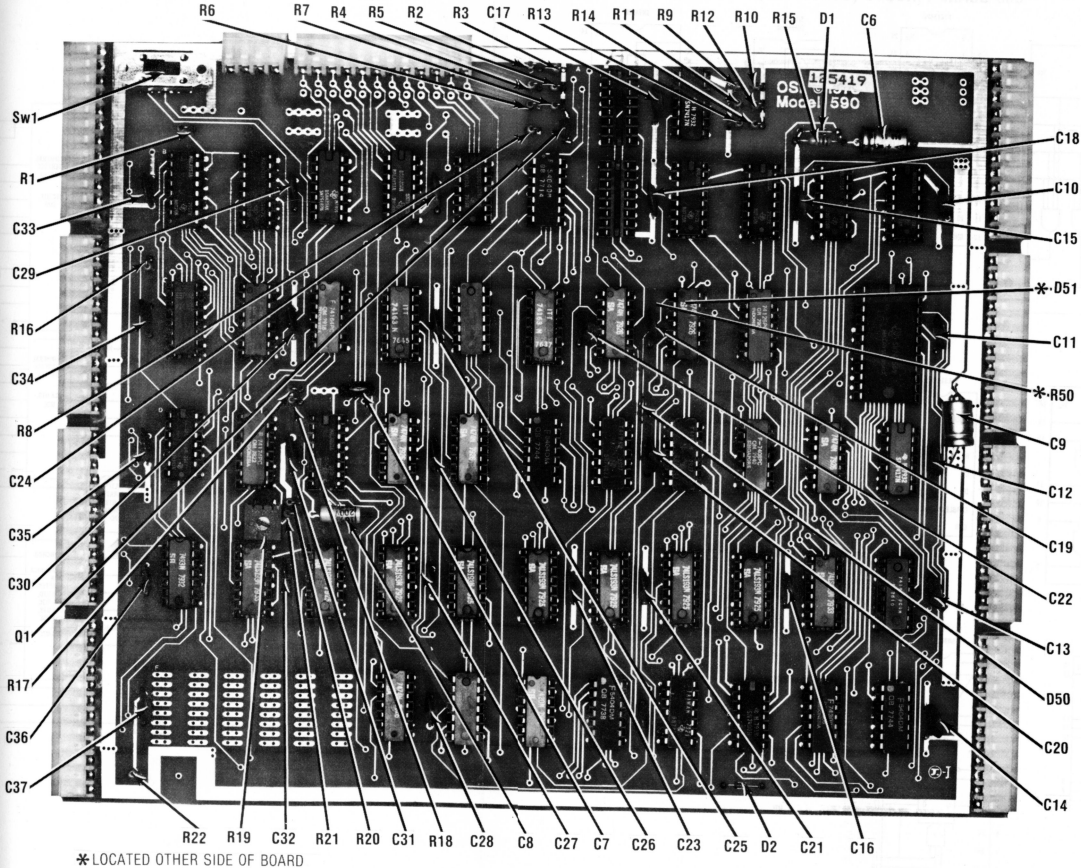
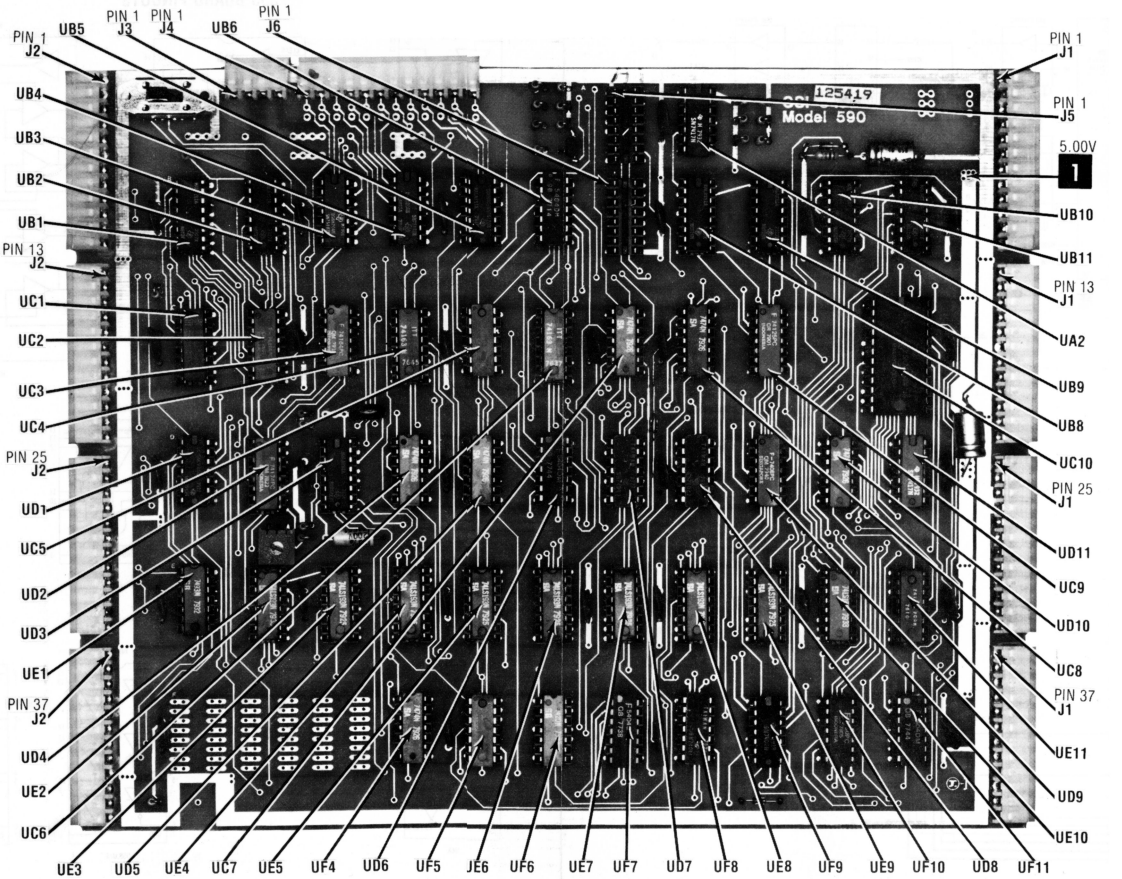


*LOCATED OTHER SIDE OF BOARD

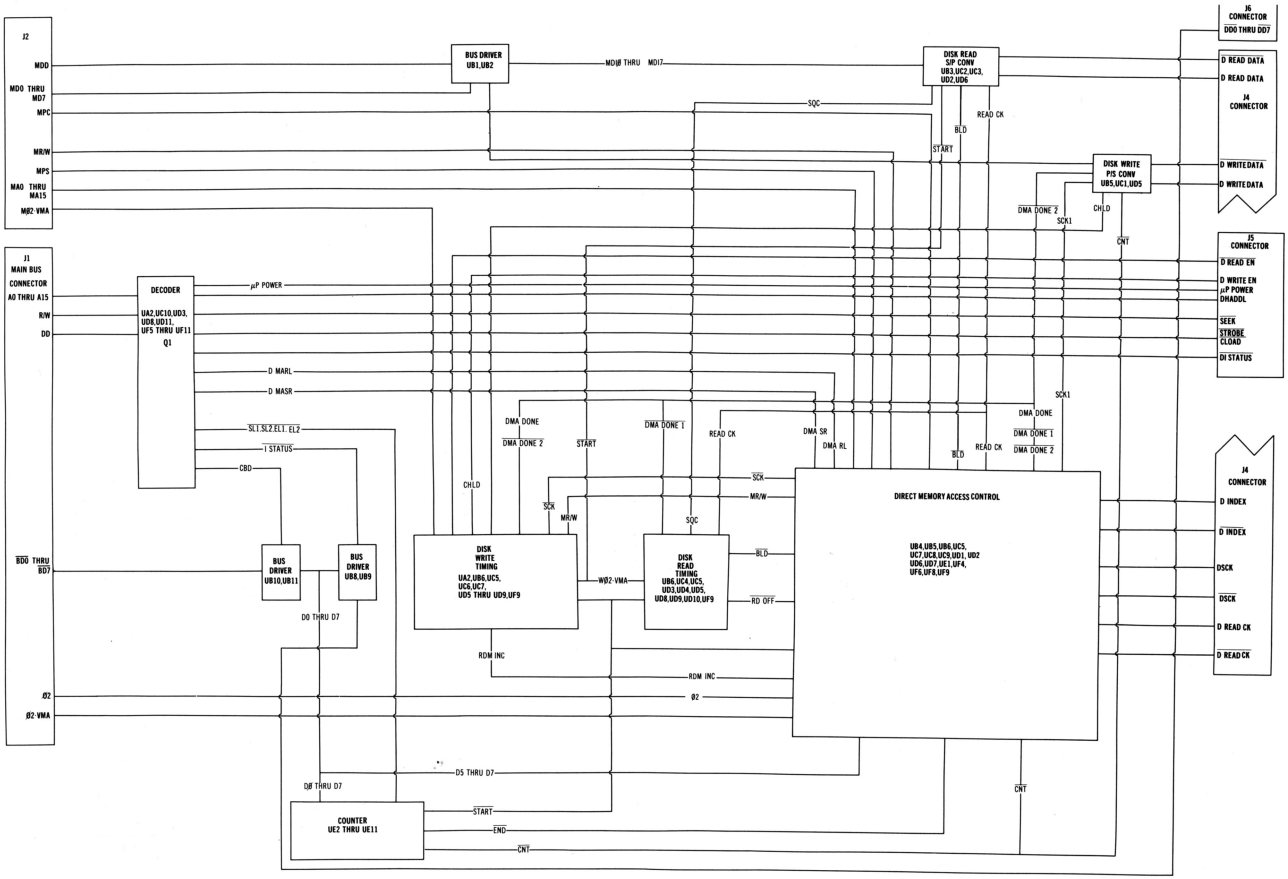
590 BOARD

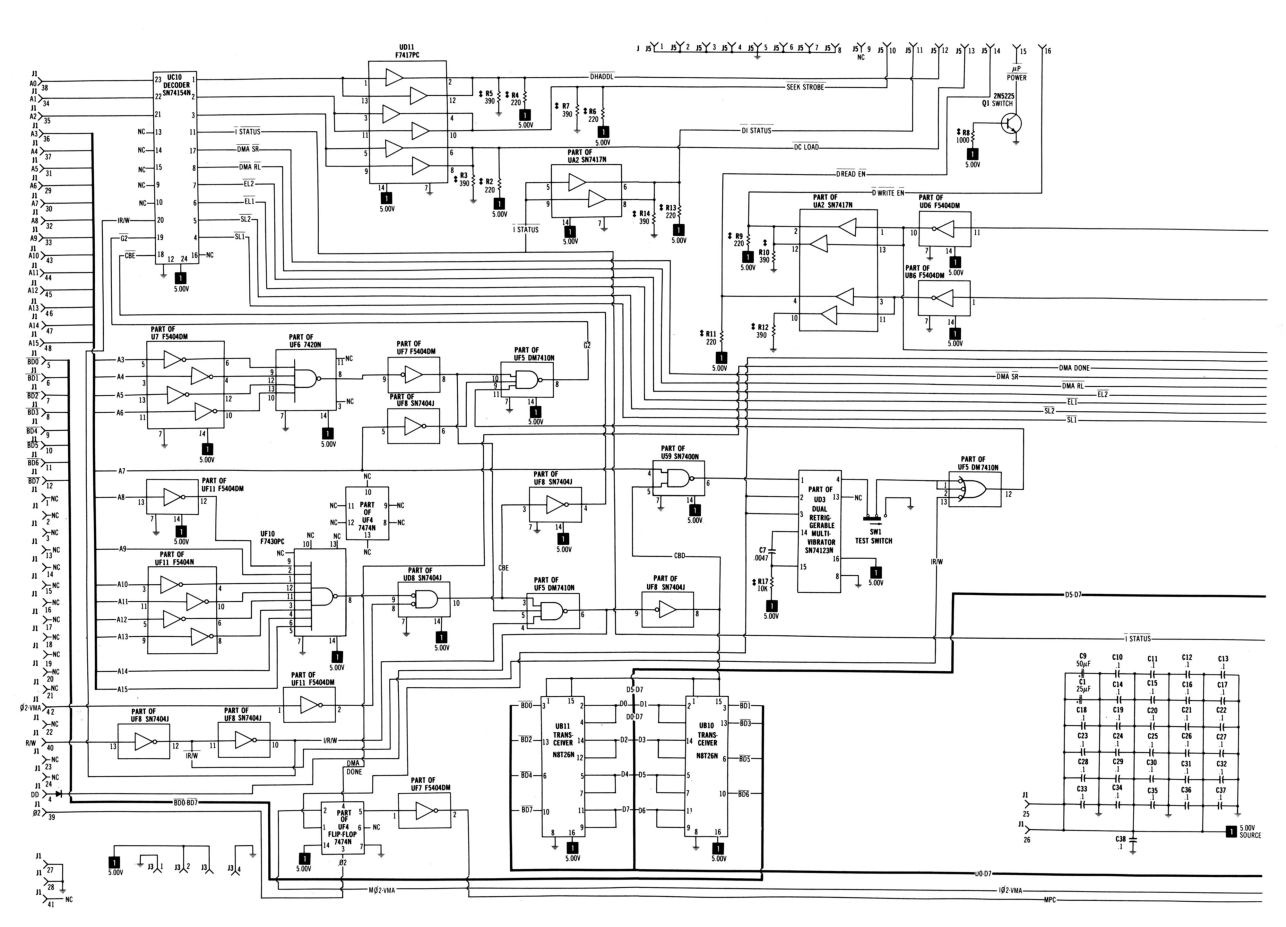
151



A Howard W. Sams CIRCUITRACE® Photo

590 BOARD

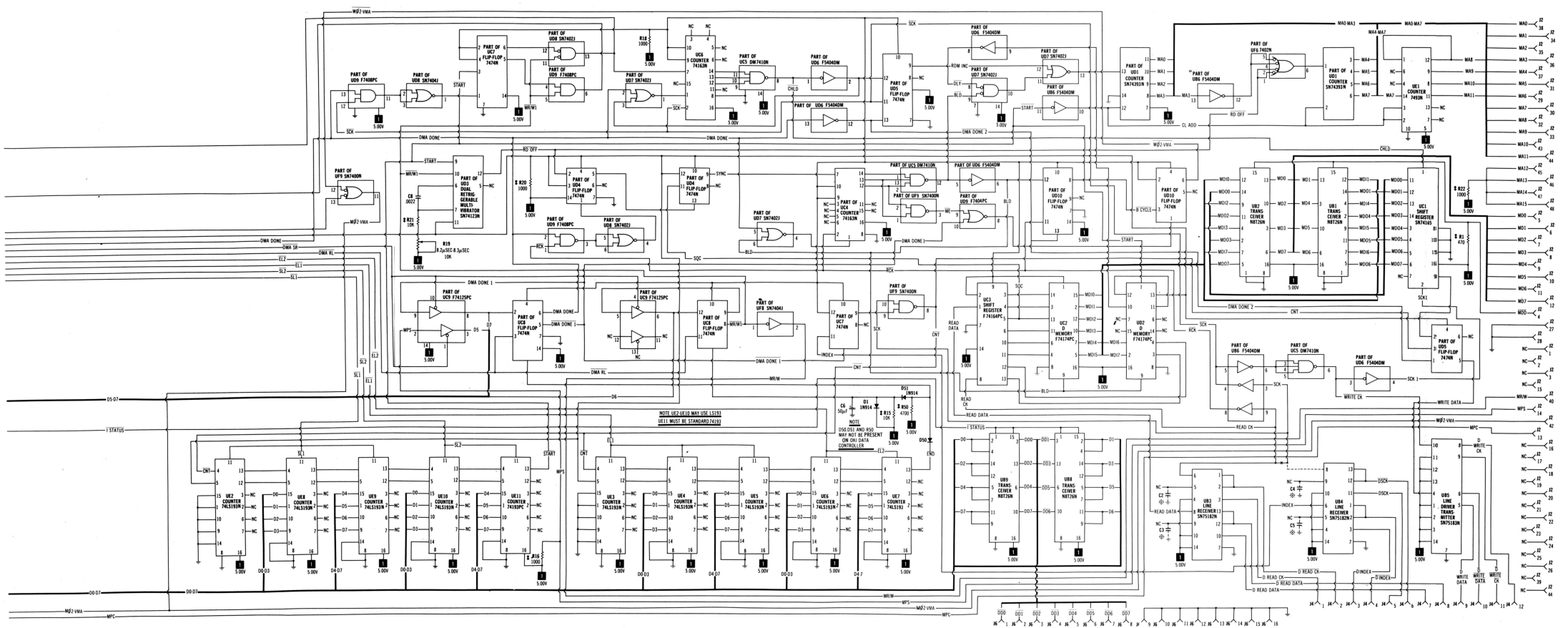

J2
MDD
MD0 THRU MD7
MPC
MR/W
MPS
MA0 THRU MA15
MB2-VMA
J1
MAIN BUS CONNECTOR
A0 THRU A15
R/W
DD
BUS DRIVER UB1,UB2
MD0 THRU MD17
SQC
DISK READ S/P CONV UB3,UC2,UC3, UD2,UD6
READ CK
BCD
START
DISK WRITE P/S CONV UB5,UC1,UD5
DMA DONE 2
SCK1
CHLD
CNT
J6 CONNECTOR
DD0 THRU DD7
J4 CONNECTOR
D READ DATA
D READ DATA
D WRITE DATA
D WRITE DATA
J5 CONNECTOR
D READ EN
D WRITE EN
μP POWER
DMADDL
SEEK
STROBE
CLOAD
DI STATUS
DECODER
UA2,UC10,UD3, UD8,UD11, UF5 THRU UF11 Q1
μP POWER
D MARL
D MASR
SL1,SL2,EL1, EL2
I STATUS
CBD
DMA DONE
DMA DONE 2
DMA DONE 1
DMA SR
DMA RL
SCK
MR/W
BUS DRIVER UB10,UB11
BUS DRIVER UB8,UB9
BD0 THRU BD7
D0 THRU D7
DISK WRITE TIMING UA2,UB6,UC5, UC6,UC7, UD5 THRU UD9,UF9
WB2-VMA
DISK READ TIMING UB6,UC4,UC5, UD3,UD4,UD5, UD8,UD9,UD10,UF9
RD OFF
DIRECT MEMORY ACCESS CONTROL
UB4,UB5,UB6,UC5, UC7,UC8,UC9,UD1, UD2 UD6,UD7,UE1,UF4, UF6,UF8,UF9
J4 CONNECTOR
D INDEX
D INDEX
DSCK
DSCK
D READ CK
D READ CK
RDM INC
Ø2
Ø2-VMA
D5 THRU D7
D8 THRU D7
COUNTER UE2 THRU UE11
START
END
CNT



A PHOTOFACT STANDARD NOTATION SCHEMATIC WITH CIRCUITRACE

FOR SCHEMATIC LEGEND AND NOTES SEE PAGES 181, 182 & REAR COVER.

590 BOARD



A PHOTOFACT STANDARD NOTATION SCHEMATIC WITH CIRCUITRACE

590 BOARD

159

FOR SCHEMATIC LEGEND AND NOTES SEE PAGES 181, 182 & REAR COVER.

160

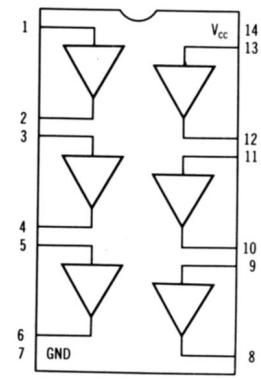
590 BOARD

161

162

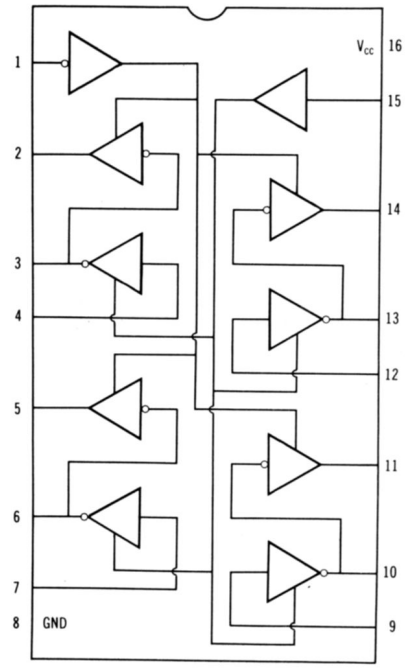
590 BOARD PINOUTS

SN7417N



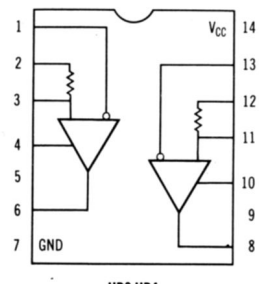
UA2,UD11

N8T26N



UB1,UB2,UB8 THRU UB11

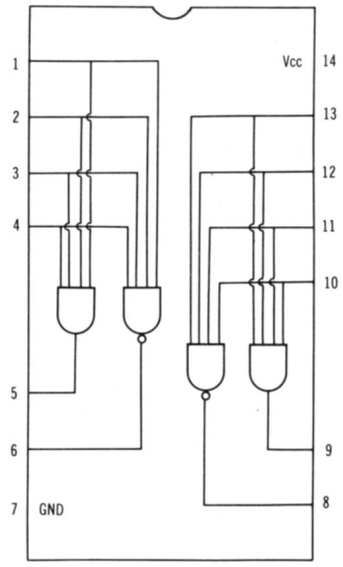
SN75182N



UB3,UB4

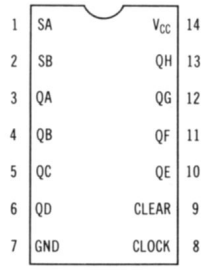
590 BOARD PINOUTS (CONTINUED)

SN75183N



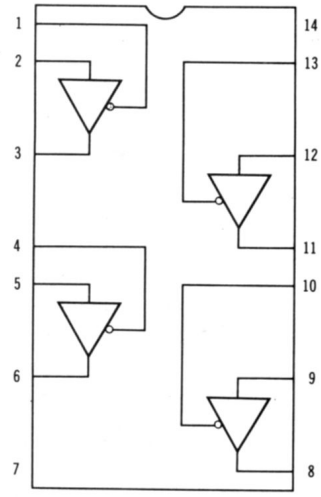
UB5

F74164PC



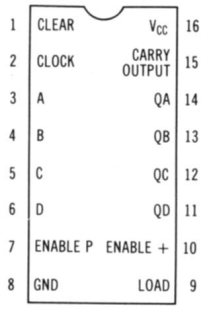
UC3

F74125PC



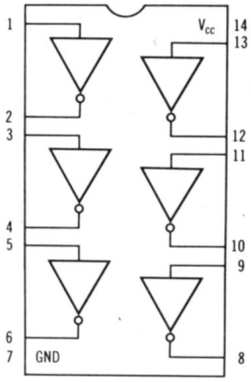
UC9

74163N



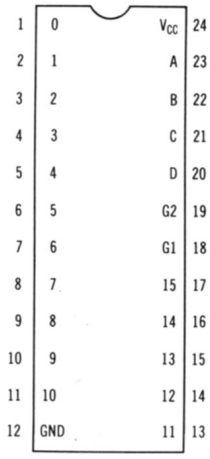
UC4,UC6

F5404DM
SN7404J



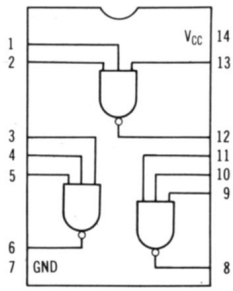
UB6,UD6,UF7,UF8,UF11

SN74154N



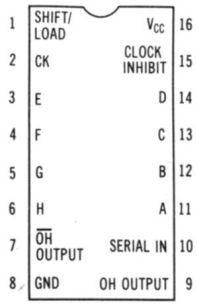
UC10

DM7410N



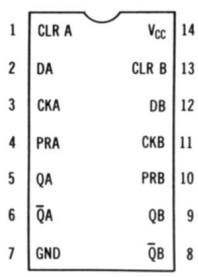
UC5,UF5

SN74165



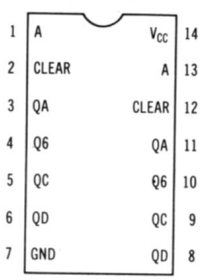
UC1

7474N



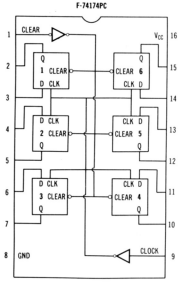
UC7,UC8,UD4,UD5, UD10,UF4

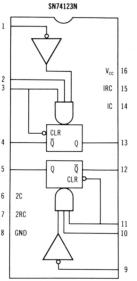
SN74393N

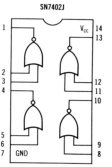


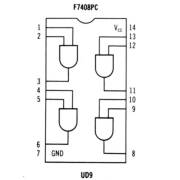
UD1

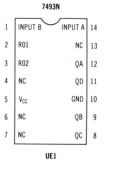
590 BOARD PINOUTS (CONTINUED)

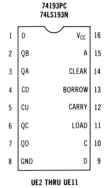


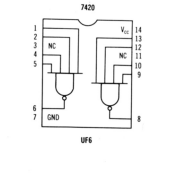


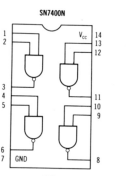


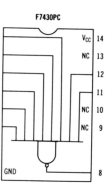


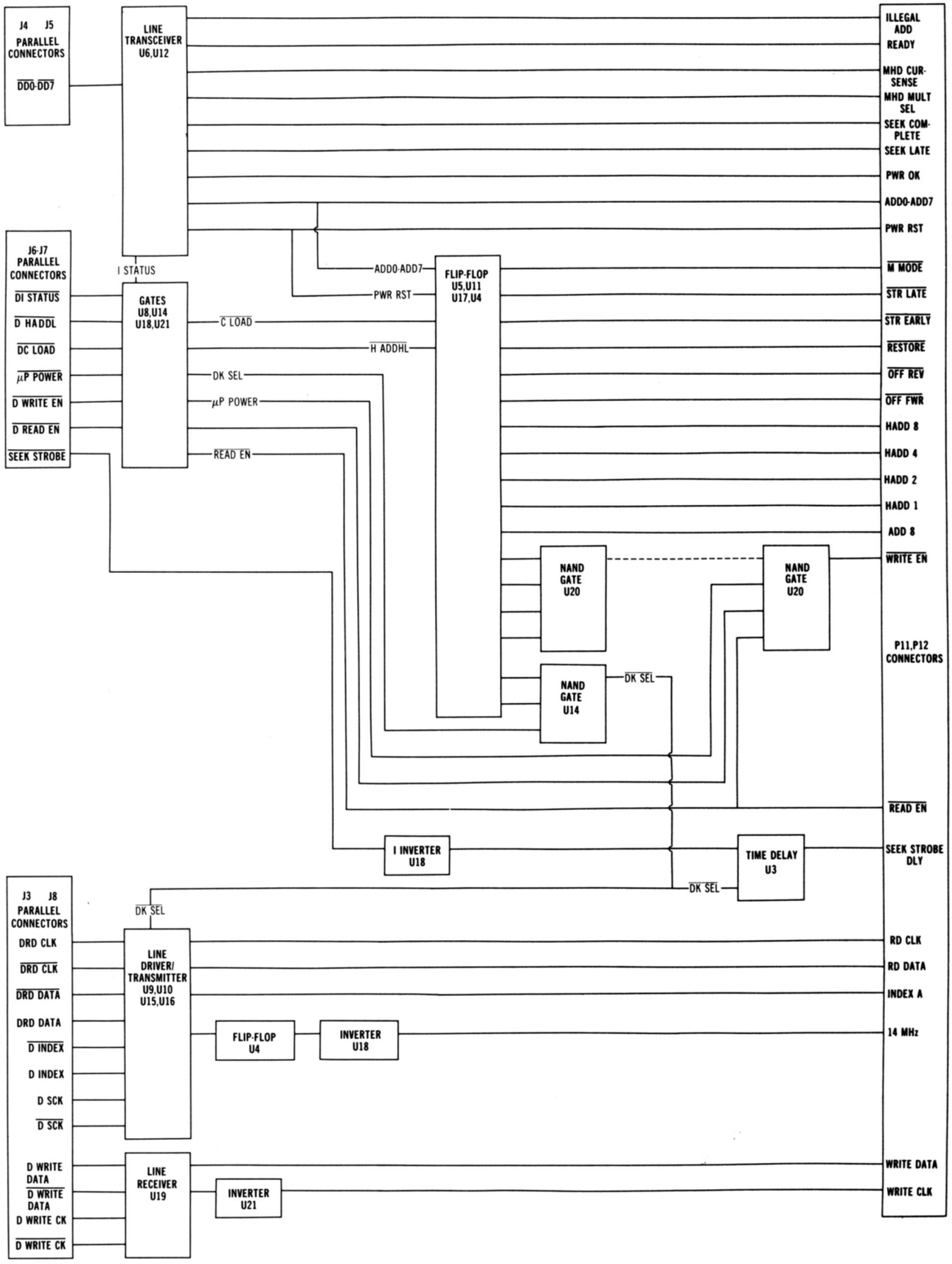








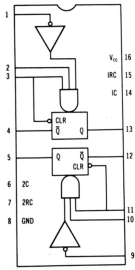




592 BOARD BLOCK

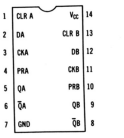
592 BOARD PINOUTS

SN74123N



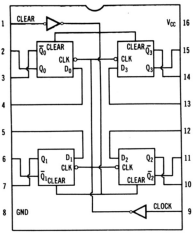
U3

SN7474N



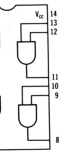
U4

DM74175N
F74175PC



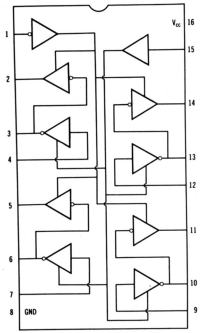
U5,U11,U17

7408N



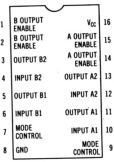
U8

N8T26AN



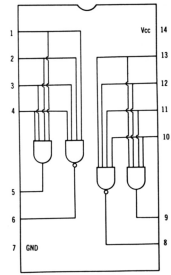
U6,U12

DS8831



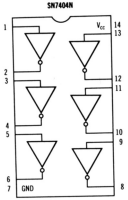
U9,U15

SN75183N



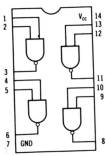
U10,U16

SN7404N



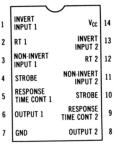
U18,U21

SN7400N



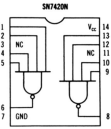
U14

SN75182N

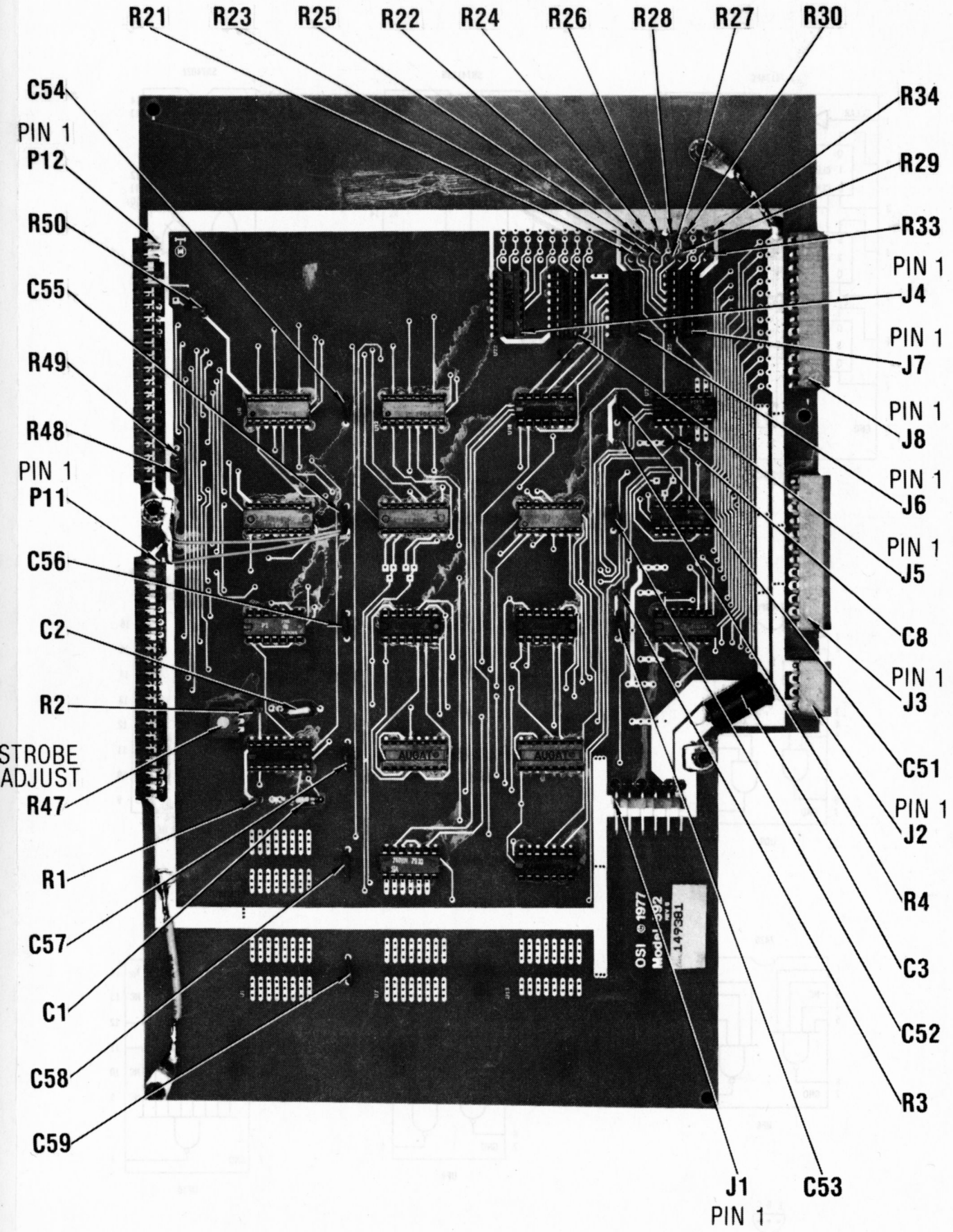


U19

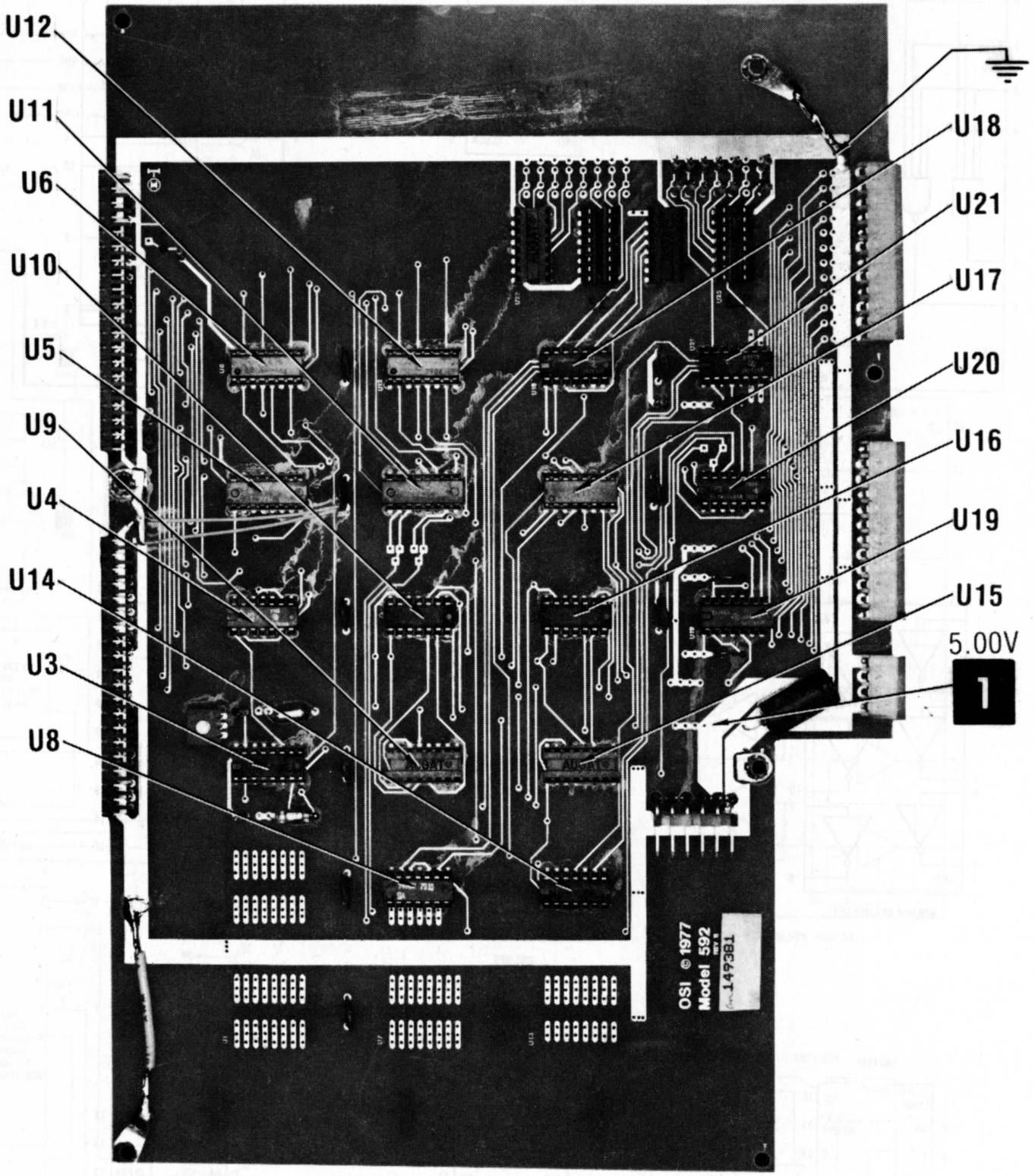
SN7420N



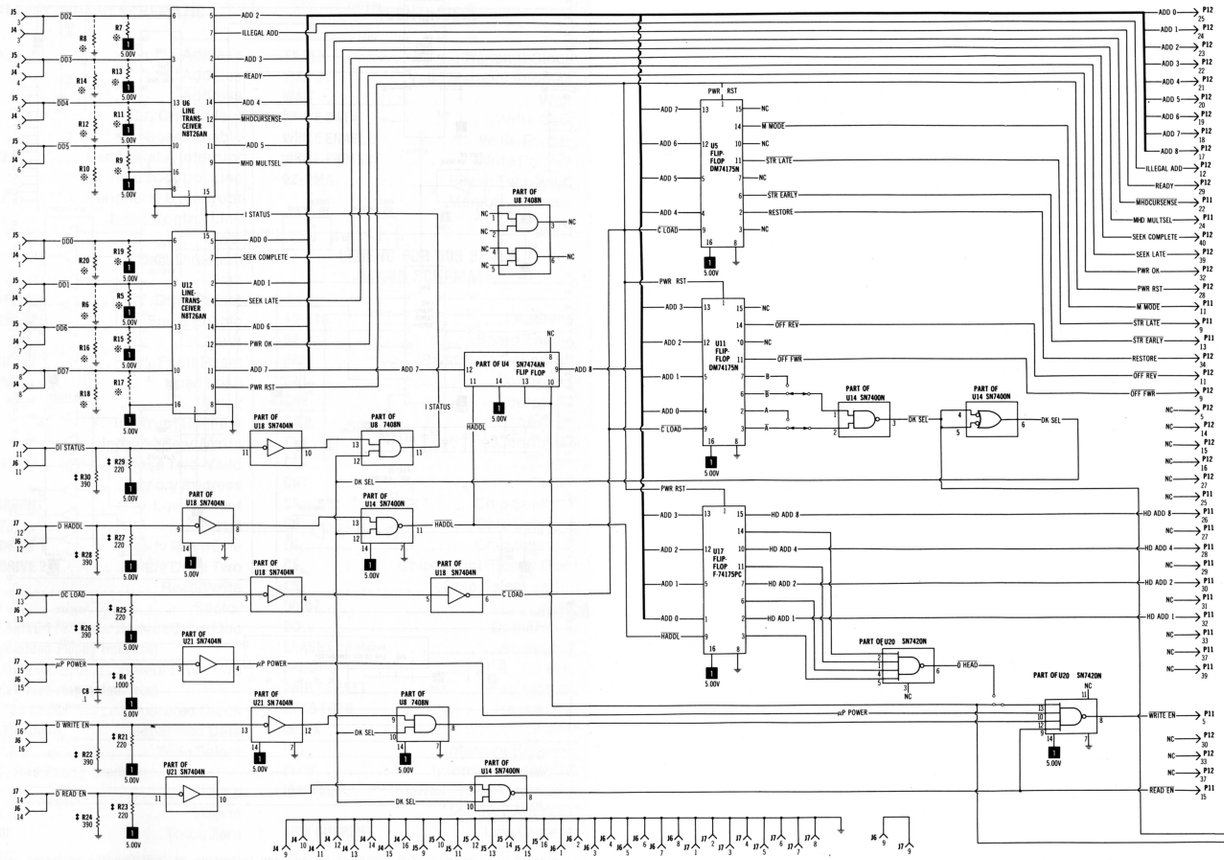
U20

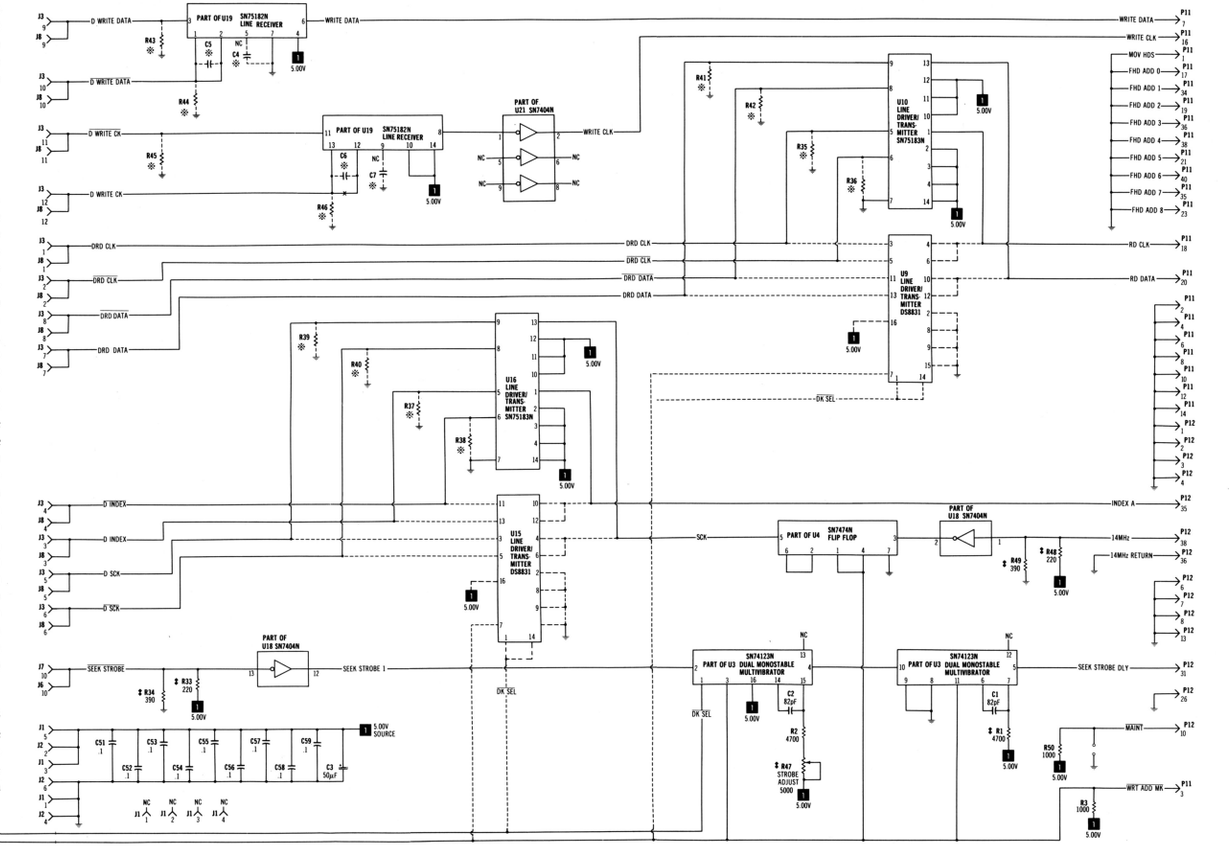

R21
R23
R25
R22
R24
R26
R28
R27
R30
C54
PIN 1
P12
R50
C55
R49
R48
PIN 1
P11
C56
C2
R2
STROBE
ADJUST
R47
R1
C57
C1
C58
C59
R34
R29
R33
PIN 1
J4
PIN 1
J7
PIN 1
J8
PIN 1
J6
PIN 1
J5
C8
PIN 1
J3
C51
PIN 1
J2
R4
C3
C52
R3
J1
PIN 1
C53
OSI © 1977
Model 592
149381

592 BOARD

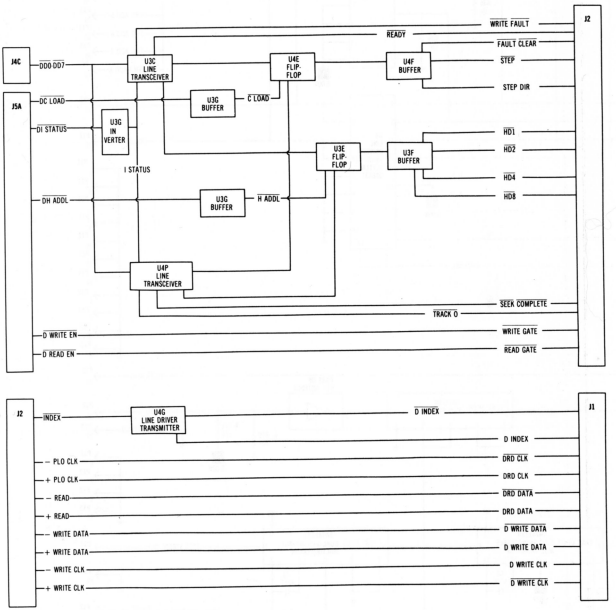


592 BOARD A Howard W. Sams CIRCUITRACE® Photo



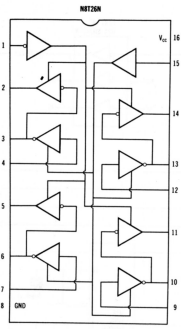


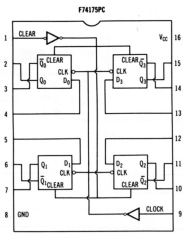
FOR SCHEMATIC LEGEND AND NOTES SEE PAGES 182 & REAR COVER.

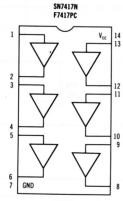

J4C
J5A
J2
DDO DD7
DC LOAD
DI STATUS
DH ADDL
D WRITE EN
D READ EN
U3C LINE TRANSCEIVER
U3G IN VERTER
I STATUS
U3G BUFFER
C LOAD
U4E FLIP-FLOP
U4F BUFFER
U3E FLIP-FLOP
U3F BUFFER
U3G BUFFER
H ADDL
U4P LINE TRANSCEIVER
WRITE FAULT
READY
FAULT CLEAR
STEP
STEP DIR
HD1
HD2
HD4
HD8
SEEK COMPLETE
TRACK 0
WRITE GATE
READ GATE

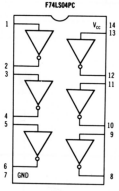
J2
J1
INDEX
U4G LINE DRIVER TRANSMITTER
D INDEX
– PLO CLK
+ PLO CLK
– READ
+ READ
– WRITE DATA
+ WRITE DATA
– WRITE CLK
+ WRITE CLK
D INDEX
DRD CLK
DRD CLK
DRD DATA
DRD DATA
D WRITE DATA
D WRITE DATA
D WRITE CLK
D WRITE CLK

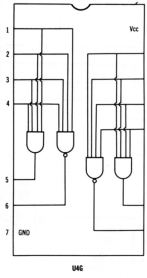
594 BOARD PINOUTS

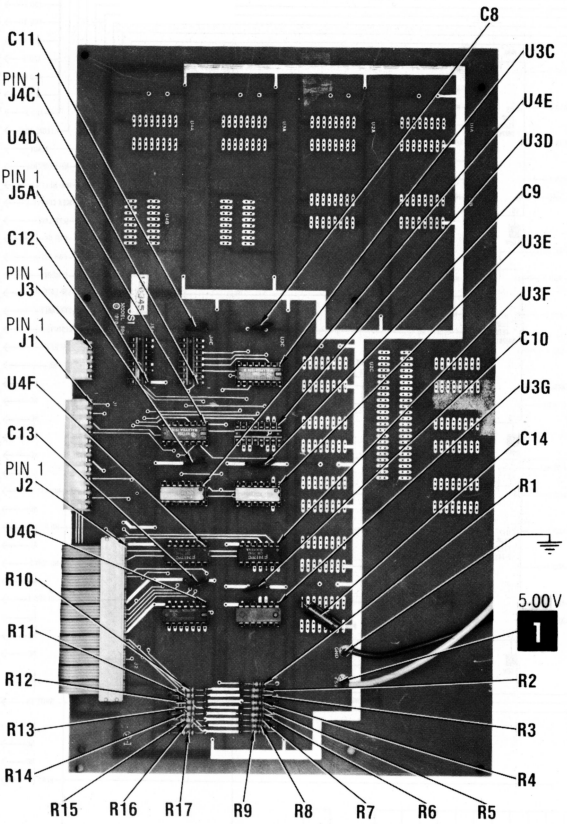






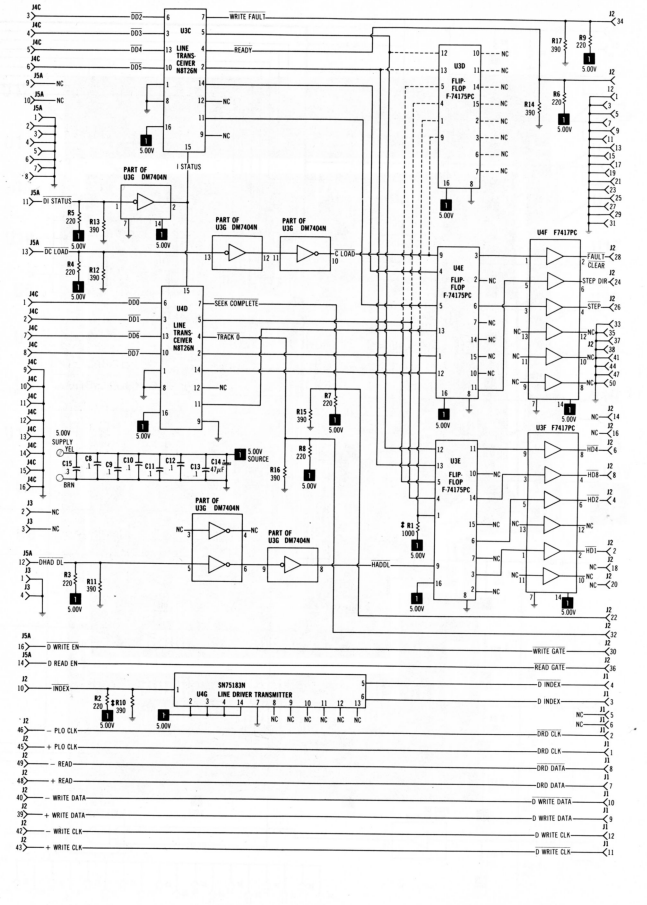






A Howard W. Sams CIRCUITRACE Photo

594 BOARD



A PHOTOFACT STANDARD NOTATION SCHEMATIC
WITH CIRCUITRACE

594 BOARD

FOR SCHEMATIC LEGEND AND NOTES SEE REAR COVER.

555 BOARD (CONTINUED)

F5XX ..... Address $F5XX_{16}$
IA0-IA9 ..... Internal Address
ID0-ID7 ..... Internal Data
IIRQ ..... Internal Interrupt Request
IRQ ..... Interrupt Request
IR/W ..... Internal Read/Write
Ø2•VMA ..... Internal Phase Two•Valid Memory Address
PAPER ..... Paper
P.F. READY ..... Paper Feed Ready
P.F.STROBE ..... Paper Feed Strobe
PORT 0 CLOCK ..... Port 0 Clock
PORT 0 IN ..... Port 0 In
PORT 0 OUT ..... Port 0 Out
PORT 1 CLOCK ..... Port 1 Clock
PORT 1 IN ..... Port 1 In
PORT 1 OUT ..... Port 1 Out
PORT 2 CLOCK ..... Port 2 Clock
PORT 2 IN ..... Port 2 In
PORT 2 OUT ..... Port 2 Out
PORT 3 CLOCK ..... Port 3 Clock
PORT 3 IN ..... Port 3 In
PORT 3 OUT ..... Port 3 Out
PORT 15 CLOCK ..... Port 15 Clock
PORT 15 IN ..... Port 15 In
PORT 15 OUT ..... Port 15 Out
PRIME ..... Prime
PRINTER READY ..... Printer Ready
P.W. READY ..... Print Wheel Ready
P.W. STROBE ..... Print Wheel Strobe
RESTORE ..... Restore
R/W ..... Read/Write
SELECT ..... Select
STROBE ..... Strobe
WAIT ..... Wait
Ø2•VMA ..... Phase Two•Valid Memory Address

LEGEND FOR 590 BOARD SCHEMATIC

A0-A15 ..... Address
B CYCLE ..... Byte Cycle
BD0-BD7 ..... Bus Data
BLD ..... Byte Load
CBD ..... Computer Bus Direction
CBE ..... Computer Bus Enable
CHLD ..... Character Load
CL ADD ..... Clear Address
CNT ..... Count
DC LOAD ..... Disk Control Load
DD ..... Data Direction
D0-D7 ..... Data
DD0-DD7 ..... Disk Data
D HADDL ..... Disk Head Address Load
D INDEX ..... Disk Index
DI STATUS ..... Disk Input Status
DLY ..... Delay
DMA DONE .. Direct Memory Access Done
DMA DONE 1 ..... Direct Memory Access Done One
DMA DONE 2 ..... Direct Memory Access Done Two
DMA RL ..... Direct Memory Access Register Load
DMA SR ..... Direct Memory Access Status Register
D READ CK ..... Disk Read Clock
D READ DATA ..... Disk Read Data
D READ EN ..... Disk Read Enable
D SCK ..... Disk Servo Clock
D WRITE CK ..... Disk Write Clock
D WRITE DATA ..... Disk Write Data
D WRITE EN ..... Disk Write Enable
EL1 ..... End Load One
EL2 ..... End Load Two
END ..... End
G2 ..... Gate Two

Any $\overline{\text{Bar}}$ above any alphabetical or numerical combination indicates line active in a low (0) state.

590 BOARD (CONTINUED)

INDEX ..... Index
IR/W ..... Internal Read/Write
I STATUS ..... Input Status
MD0-MD7 ..... Memory Data
MA0-MA15 ..... Memory Address
MDD ..... Memory Data Direction
MDI0-MDI7 ..... Memory Data In
MD00-MD07 ..... Memory Data Out
MPC ..... Memory Process Clear
MPS ..... Memory Process Set
MR/W ..... Memory Read/Write
MR/W1 ..... Memory Read/Write One
ME ..... Memory Enable
MØ2·VMA ..... Memory Phase Two·Valid Memory Address
PD ..... Partial Decode
RD OFF ..... Read Offset
READ CK ..... Read Clock
READ DATA ..... Read Data
RDM INC ..... Read Memory Increment
RCK ..... Read Clock
SCK ..... Servo Clock
SCK1 ..... Servo Clock One
SEEK STROBE ..... Seek Strobe
SL1 ..... Start Load One
SL2 ..... Start Load Two
START ..... Start
SQC ..... Sync QC
SYNC ..... Sync
WRITE DATA ..... Write Data
WØ2·VMA ..... Write Phase Two·Valid Memory Address
μP POWER ..... Microprocessor Power
Ø2 ..... Phase Two
Ø2·VMA ..... Phase Two·Valid Memory Address

LEGEND FOR 592 BOARD SCHEMATIC

A ..... Disk Address A
ADD0-ADD8 ..... Address Disk
B ..... Disk Address B
C LOAD ..... Control Load
DC LOAD ..... Disk Control Load
DD0-DD7 ..... Disk Data
D HADDL ..... Disk Head Address Load
D INDEX ..... Disk Index
DI STATUS ..... Disk Input Status
DK SEL ..... Disk Select
DRD CLK ..... Disk Read Clock
DRD DATA ..... Disk Read Data
D READ EN ..... Disk Read Enable
D SCK ..... Disk Servo Clock
D WRITE CLK ..... Disk Write Clock
D WRITE DATA ..... Disk Write Data
D WRITE EN ..... Disk Write Enable
FHDADD0-FHDADD8 .. Fixed Head Address
HADDL ..... Head Address Load
HDADD1 ... Head Selection Address Line
HDADD2 ... Head Selection Address Line
HDADD4 ... Head Selection Address Line
HDADD8 ... Head Selection Address Line
ILLEGAL ADD ..... Illegal Address
INDEX A ..... Index A
I STATUS ..... Input Status
MAINT ..... Maintenance
MHDCURSENSE ..... Moving Head Current Sense
MHD MULTSEL ..... Multiple Moving Head Selected
M MODE ..... Maintenance Mode
MOV HDS ..... Moving Heads
OFF FWR ..... Offset Forward
OFF REV ..... Offset Reverse
PWR OK ..... Power OK

Any $\overline{\text{Bar}}$ above any alphabetical or numerical combination indicates line active in a low (0) state.

592 BOARD (CONTINUED)

PWR RST ..... Power Reset
RDCLK ..... Read Clock
RDDATA ..... Read Data
READ EN ..... Read Enable
READY ..... Ready
RESTORE ..... Restore
SCK ..... Servo Clock
SEEK COMPLETE ..... Seek Complete
SEEK LATE ..... Seek Late
SEEK STROBE ..... Seek Strobe
SEEK STROBE DLY ... Seek Strobe Delayed
SEEK STROBE 1 ..... Seek Strobe One
STR EARLY ..... Strobe Early
STR LATE ..... Strobe Late
μP POWER ..... Microprocessor Power
WRITE CLK ..... Write Clock
WRITE DATA ..... Write Data
WRITE EN ..... Write Enable
WRT ADD MK ..... Write Address Mark
0 HEAD ..... Zero Head

LEGEND FOR 594 BOARD SCHEMATIC

C LOAD ..... Control Load
D INDEX ..... Disk Index
D HADDL ..... Disk Head Address Load
D READ EN ..... Disk Read Enable
D WRITE CLK ..... Disk Write Clock
D WRITE DATA ..... Disk Write Data
D WRITE EN ..... Disk Write Enable
DC LOAD ..... Disk Control Load

594 BOARD (CONTINUED)

DD0-DD7 ..... Disk Data
DI STATUS ..... Disk Input Status
DRD CLK ..... Disk Read Clock
DRD DATA ..... Disk Read Data
FAULT CLEAR ..... Fault Clear
HADDL ..... Head Address Load
HD1,HD2,HD4,HD8 ..... Head Selection Address Lines
I STATUS ..... Input Status
PLO CLK ..... Phase Lock Osc Clock
READY ..... Ready
SEEK COMPLETE ..... Seek Complete
STEP DIR ..... Step Direction
TRACK 0 ..... Track Zero
WRITE CLK ..... Write Clock
WRITE FAULT ..... Write Fault

SCHEMATIC NOTES

—✕— Circuitry not used in some versions.
– – – Circuitry used in some versions.
※ Optional part. Value determined by application
⏚ Ground
▽ Common tie point
Chassis
Flame retardant resistor
⊖ See parts list

Item numbers in rectangles appear in the alignment/adjustment instructions.
Supply voltage maintained as shown in input.
Voltages measured with digital meter.
Terminal indentification may not be found on unit.
Resistors are ¼W or less, 5% unless noted.
Value in ( ) used in some versions.

Any $\overline{\text{Bar}}$ above any alphabetical or numerical combination indicates line active in a low (0) state.